SSD0323

Advance Information

128 x 80, 16 Gray Scale Dot Matrix
OLED/PLED Segment/Common Driver with Controller

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GENERAL DESCRIPTION

SSD0323 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SSD0323 consists of 208 high voltage/current driving output pins for driving 128 segments and 80 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD0323 displays data directly from its internal 128x80x4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

SSD0323 has a 128-step contrast control and a 16 gray level control. The embedded on-chip oscillator and DC-DC voltage converter reduce the number of external components.

FEATURES

- Support max. 128 x 80 matrix panel
- Power supply: VDD=2.4V - 3.5V
  VCC=8.0V - 16.0V
- OLED driving output voltage, 14V maximum
- DC-DC voltage converter
- Segment maximum source current: 300uA
- Common maximum sink current: 40mA
- Embedded 128 x 80 x 4 bit SRAM display memory
- External current reference
- 128 step contrast control on monochrome passive OLED panel
- 16 gray scale
- On-Chip Oscillator
- Programmable Frame Rate/Pre-charge voltage and segment low voltage (VSL)
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Row re-mapping and Column re-mapping
- Low power consumption (<5.0uA @sleep mode)
- Wide range of operating temperature: -40 to 85 °C

ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference
SSD0323Z	128	80	COG	Page 7

BLOCK DIAGRAM

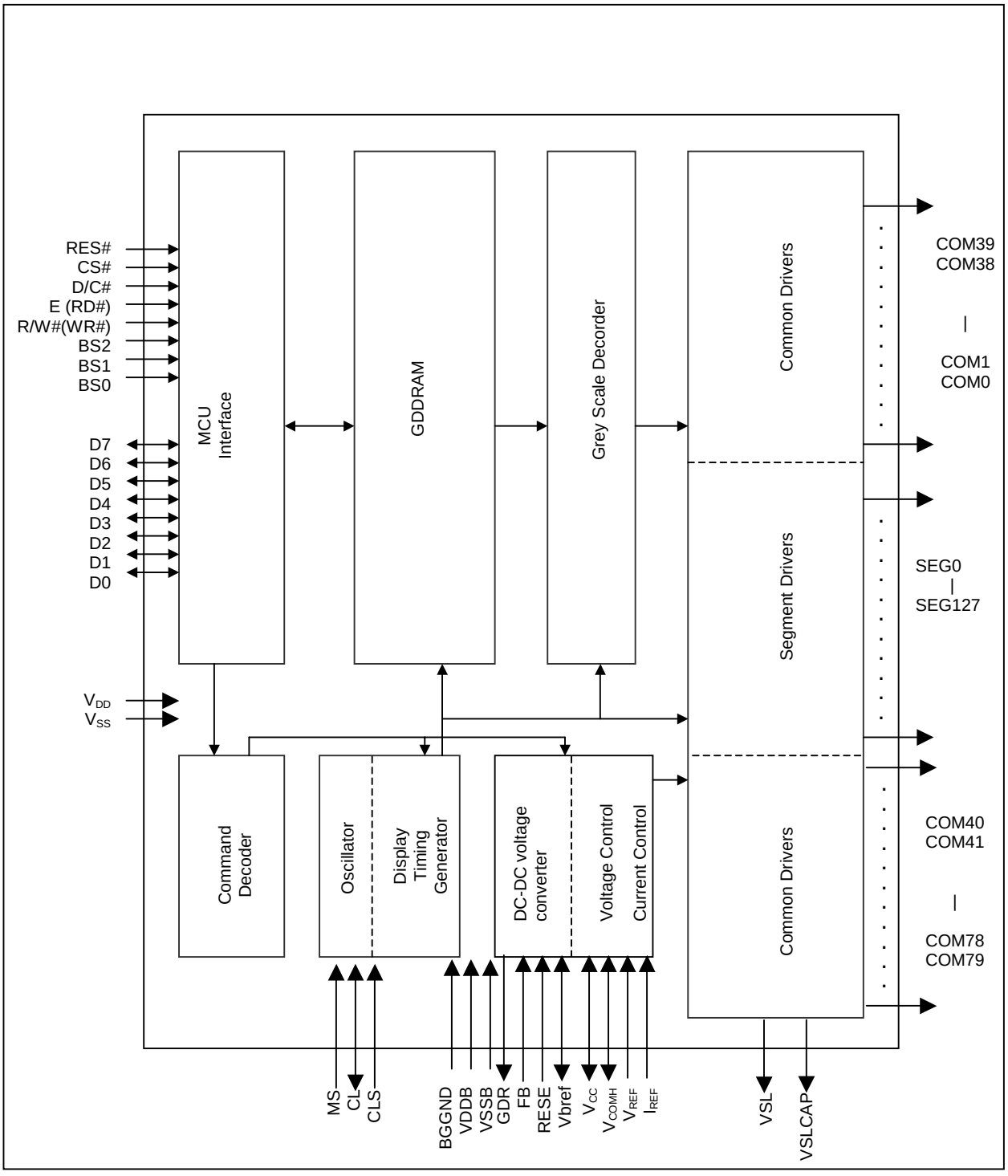
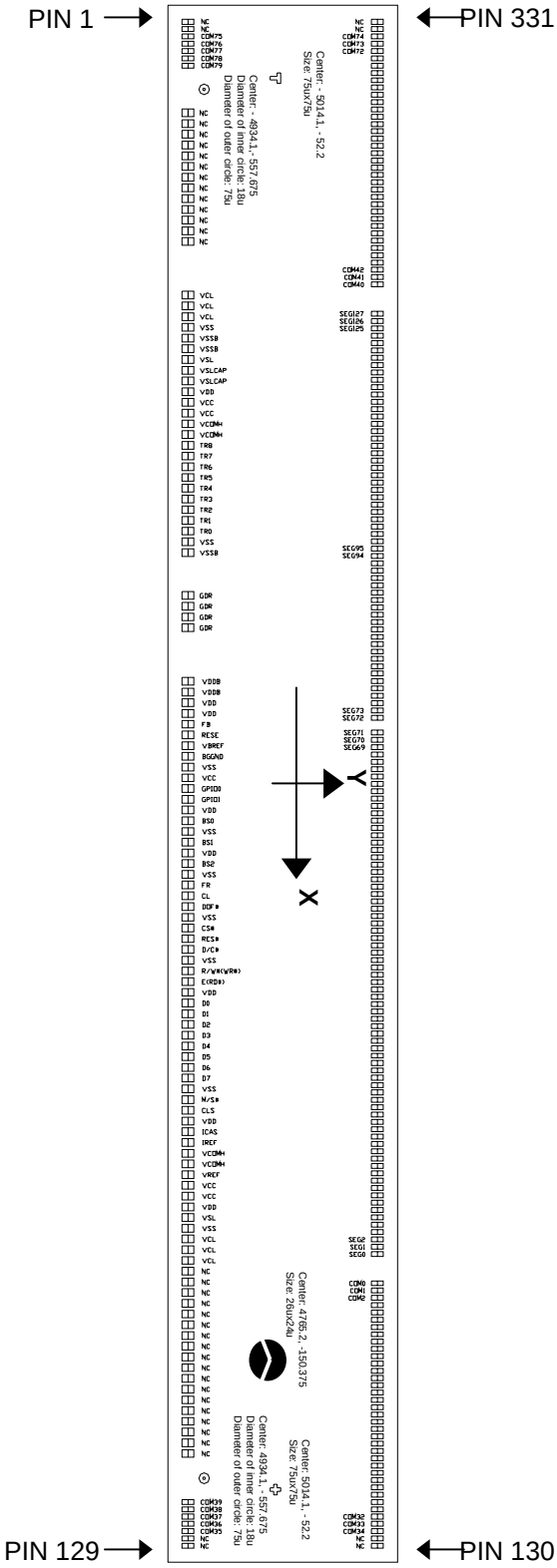


Figure 1 - Block Diagram

SSD0323Z GOLD BUMP DIE PAD ASSIGNMENT



+ represents the centre of the alignment mark

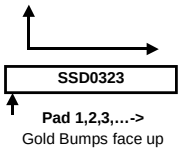
TR0-TR8, GPIO0, GPIO1, ICAS
These are reserved pins. No connection should be made for these pins and left float individually.

Die Size: 11022um x 1588um
Die Thickness: 457 +/- 25um
I/O pad pitch (a): 76.2um
SEG pad pitch (b): 52.2um
COM pad pitch (c): 51.8um
Bump Height: Nominal 18um

Figure 2 - SSD0323Z Gold bump die pad assignment

SSD0323Z Die Pad Coordinates

Pad#	Signal	X-pos	Y-pos
1	DUMMY	-5414.000	-672.075
2	DUMMY	-5361.800	-672.075
3	COM75	-5309.600	-672.075
4	COM76	-5257.800	-672.075
5	COM77	-5206.000	-672.075
6	COM78	-5154.200	-672.075
7	COM79	-5102.400	-672.075
8	DUMMY	-4767.075	-672.075
9	DUMMY	-4690.875	-672.075
10	DUMMY	-4614.675	-672.075
11	DUMMY	-4538.475	-672.075
12	DUMMY	-4462.275	-672.075
13	DUMMY	-4386.075	-672.075
14	DUMMY	-4309.875	-672.075
15	DUMMY	-4233.675	-672.075
16	DUMMY	-4157.475	-672.075
17	DUMMY	-4081.275	-672.075
18	DUMMY	-4005.075	-672.075
19	DUMMY	-3928.875	-672.075
20	DUMMY	-3852.675	-672.075
21	VCL	-3471.675	-672.075
22	VCL	-3395.475	-672.075
23	VCL	-3319.275	-672.075
24	VSS	-3243.075	-672.075
25	VSSB	-3166.875	-672.075
26	VSSB	-3090.675	-672.075
27	VSL	-3014.475	-672.075
28	VSLCAP	-2938.275	-672.075
29	VSLCAP	-2862.075	-672.075
30	VDD	-2785.875	-672.075
31	VCC	-2709.675	-672.075
32	VCC	-2633.475	-672.075
33	VCOMH	-2557.275	-672.075
34	VCOMH	-2481.075	-672.075
35	TR8	-2404.875	-672.075
36	TR7	-2328.675	-672.075
37	TR6	-2252.475	-672.075
38	TR5	-2176.275	-672.075
39	TR4	-2100.075	-672.075
40	TR3	-2023.875	-672.075
41	TR2	-1947.675	-672.075
42	TR1	-1871.475	-672.075
43	TR0	-1795.275	-672.075
44	VSS	-1719.075	-672.075
45	VSSB	-1642.875	-672.075
46	GDR	-1338.075	-672.075
47	GDR	-1261.875	-672.075
48	GDR	-1185.675	-672.075
49	GDR	-1109.475	-672.075
50	VDDB	-728.475	-672.075
51	VDDB	-652.275	-672.075
52	VDD	-576.075	-672.075
53	VDD	-499.875	-672.075
54	FB	-423.675	-672.075
55	RESE	-347.475	-672.075
56	VBREF	-271.275	-672.075
57	BGGND	-195.075	-672.075
58	VSS	-118.875	-672.075
59	VCC	-42.675	-672.075
60	GPIO0	33.525	-672.075
61	GPIO1	109.725	-672.075
62	VDD	185.925	-672.075
63	BS0	262.125	-672.075
64	VSS	338.325	-672.075
65	BS1	414.525	-672.075
66	VDD	490.725	-672.075
67	BS2	566.925	-672.075
68	VSS	643.125	-672.075
69	FR	719.325	-672.075
70	CL	795.525	-672.075
71	DOF#	871.725	-672.075
72	VSS	947.925	-672.075
73	CS#	1024.125	-672.075
74	RES#	1100.325	-672.075
75	D/C#	1176.525	-672.075
76	VSS	1252.725	-672.075
77	R/W#(WR#)	1328.925	-672.075
78	E(RD#)	1405.125	-672.075
79	VDD	1481.325	-672.075
80	D0	1557.525	-672.075
81	D1	1633.725	-672.075
82	D2	1709.925	-672.075
83	D3	1786.125	-672.075
84	D4	1862.325	-672.075
85	D5	1938.525	-672.075
86	D6	2014.725	-672.075
87	D7	2090.925	-672.075
88	VSS	2167.125	-672.075
89	M/S#	2243.325	-672.075
90	CLS	2319.525	-672.075
91	VDD	2395.725	-672.075
92	ICAS	2471.925	-672.075
93	IREF	2548.125	-672.075
94	VCOMH	2624.325	-672.075
95	VCOMH	2700.525	-672.075
96	VREF	2776.725	-672.075
97	VCC	2852.925	-672.075
98	VCC	2929.125	-672.075
99	VDD	3005.325	-672.075
100	VSL	3081.525	-672.075
101	VSS	3157.725	-672.075
102	VCL	3233.925	-672.075
103	VCL	3310.125	-672.075
104	VCL	3386.325	-672.075
105	DUMMY	3462.525	-672.075
106	DUMMY	3538.725	-672.075
107	DUMMY	3614.925	-672.075
108	DUMMY	3691.125	-672.075
109	DUMMY	3767.325	-672.075
110	DUMMY	3843.525	-672.075
111	DUMMY	3919.725	-672.075
112	DUMMY	3995.925	-672.075
113	DUMMY	4072.125	-672.075
114	DUMMY	4148.325	-672.075
115	DUMMY	4224.525	-672.075
116	DUMMY	4300.725	-672.075
117	DUMMY	4376.925	-672.075
118	DUMMY	4453.125	-672.075
119	DUMMY	4529.325	-672.075
120	DUMMY	4605.525	-672.075
121	DUMMY	4681.725	-672.075
122	DUMMY	4757.925	-672.075
123	COM39	5102.400	-672.075
124	COM38	5154.200	-672.075
125	COM37	5206.000	-672.075
126	COM36	5257.800	-672.075
127	COM35	5309.600	-672.075
128	DUMMY	5361.800	-672.075
129	DUMMY	5414.000	-672.075
130	DUMMY	5414.000	672.075
131	DUMMY	5361.800	672.075
132	COM34	5309.600	672.075
133	COM33	5257.800	672.075
134	COM32	5206.000	672.075
135	COM31	5154.200	672.075
136	COM30	5102.400	672.075
137	COM29	5050.600	672.075
138	COM28	4998.800	672.075
139	COM27	4947.000	672.075
140	COM26	4895.200	672.075
141	COM25	4843.400	672.075
142	COM24	4791.600	672.075
143	COM23	4739.800	672.075
144	COM22	4688.000	672.075
145	COM21	4636.200	672.075
146	COM20	4584.400	672.075
147	COM19	4532.600	672.075
148	COM18	4480.800	672.075
149	COM17	4429.000	672.075
150	COM16	4377.200	672.075
151	COM15	4325.400	672.075
152	COM14	4273.600	672.075
153	COM13	4221.800	672.075
154	COM12	4170.000	672.075
155	COM11	4118.200	672.075
156	COM10	4066.400	672.075
157	COM9	4014.600	672.075
158	COM8	3962.800	672.075
159	COM7	3911.000	672.075
160	COM6	3859.200	672.075
161	COM5	3807.400	672.075
162	COM4	3755.600	672.075
163	COM3	3703.800	672.075
164	COM2	3652.000	672.075
165	COM1	3600.200	672.075
166	COM0	3548.400	672.075
167	SEG0	3340.800	672.075
168	SEG1	3288.600	672.075
169	SEG2	3236.400	672.075
170	SEG3	3184.200	672.075
171	SEG4	3132.000	672.075
172	SEG5	3079.800	672.075
173	SEG6	3027.600	672.075
174	SEG7	2975.400	672.075
175	SEG8	2923.200	672.075
176	SEG9	2871.000	672.075
177	SEG10	2818.800	672.075
178	SEG11	2766.600	672.075
179	SEG12	2714.400	672.075
180	SEG13	2662.200	672.075
181	SEG14	2610.000	672.075
182	SEG15	2557.800	672.075
183	SEG16	2505.600	672.075
184	SEG17	2453.400	672.075
185	SEG18	2401.200	672.075
186	SEG19	2349.000	672.075
187	SEG20	2296.800	672.075
188	SEG21	2244.600	672.075
189	SEG22	2192.400	672.075
190	SEG23	2140.200	672.075
191	SEG24	2088.000	672.075
192	SEG25	2035.800	672.075
193	SEG26	1983.600	672.075
194	SEG27	1931.400	672.075
195	SEG28	1879.200	672.075
196	SEG29	1827.000	672.075
197	SEG30	1774.800	672.075
198	SEG31	1722.600	672.075
199	SEG32	1670.400	672.075
200	SEG33	1618.200	672.075
201	SEG34	1566.000	672.075
202	SEG35	1513.800	672.075
203	SEG36	1461.600	672.075
204	SEG37	1409.400	672.075
205	SEG38	1357.200	672.075
206	SEG39	1305.000	672.075
207	SEG40	1252.800	672.075
208	SEG41	1200.600	672.075
209	SEG42	1148.400	672.075
210	SEG43	1096.200	672.075
211	SEG44	1044.000	672.075
212	SEG45	991.800	672.075
213	SEG46	939.600	672.075
214	SEG47	887.400	672.075
215	SEG48	835.200	672.075
216	SEG49	783.000	672.075
217	SEG50	730.800	672.075
218	SEG51	678.600	672.075
219	SEG52	626.400	672.075
220	SEG53	574.200	672.075
221	SEG54	522.000	672.075
222	SEG55	469.800	672.075
223	SEG56	417.600	672.075
224	SEG57	365.400	672.075
225	SEG58	313.200	672.075
226	SEG59	261.000	672.075
227	SEG60	208.800	672.075
228	SEG61	156.600	672.075
229	SEG62	104.400	672.075
230	SEG63	52.200	672.075
231	SEG64	0.000	672.075
232	SEG65	-52.200	672.075
233	SEG66	-104.400	672.075
234	SEG67	-156.600	672.075
235	SEG68	-208.800	672.075
236	SEG69	-261.000	672.075
237	SEG70	-313.200	672.075
238	SEG71	-365.400	672.075
239	SEG72	-469.800	672.075
240	SEG73	-522.000	672.075
241	SEG74	-574.200	672.075
242	SEG75	-626.400	672.075
243	SEG76	-678.600	672.075
244	SEG77	-730.800	672.075
245	SEG78	-783.000	672.075
246	SEG79	-835.200	672.075
247	SEG80	-887.400	672.075
248	SEG81	-939.600	672.075
249	SEG82	-991.800	672.075
250	SEG83	-1044.000	672.075
251	SEG84	-1096.200	672.075
252	SEG85	-1148.400	672.075
253	SEG86	-1200.600	672.075
254	SEG87	-1252.800	672.075
255	SEG88	-1305.000	672.075
256	SEG89	-1357.200	672.075
257	SEG90	-1409.400	672.075
258	SEG91	-1461.600	672.075
259	SEG92	-1513.800	672.075
260	SEG93	-1566.000	672.075
261	SEG94	-1618.200	672.075
262	SEG95	-1670.400	672.075
263	SEG96	-1722.600	672.075
264	SEG97	-1774.800	672.075
265	SEG98	-1827.000	672.075
266	SEG99	-1879.200	672.075
267	SEG100	-1931.400	672.075
268	SEG101	-1983.600	672.075
269	SEG102	-2035.800	672.075
270	SEG103	-2088.000	672.075
271	SEG104	-2140.200	672.075
272	SEG105	-2192.400	672.075
273	SEG106	-2244.600	672.075
274	SEG107	-2296.800	672.075
275	SEG108	-2349.000	672.075
276	SEG109	-2401.200	672.075
277	SEG110	-2453.400	672.075
278	SEG111	-2505.600	672.075
279	SEG112	-2557.800	672.075
280	SEG113	-2610.000	672.075
281	SEG114	-2662.200	672.075
282	SEG115	-2714.400	672.075
283	SEG116	-2766.600	672.075
284	SEG117	-2818.800	672.075
285	SEG118	-2871.000	672.075
286	SEG119	-2923.200	672.075
287	SEG120	-2975.400	672.075
288	SEG121	-3027.600	672.075
289	SEG122	-3079.800	672.075
290	SEG123	-3132.000	672.075
291	SEG124	-3184.200	672.075
292	SEG125	-3236.400	672.075
293	SEG126	-3288.600	672.075
294	SEG127	-3340.800	672.075
295	COM40	-3548.400	672.075
296	COM41	-3600.200	672.075
297	COM42	-3652.000	672.075
298	COM43	-3703.800	672.075
299	COM44	-3755.600	672.075
300	COM45	-3807.400	672.075
301	COM46	-3859.200	672.075
302	COM47	-3911.000	672.075
303	COM48	-3962.800	672.075
304	COM49	-4014.600	672.075
305	COM50	-4066.400	672.075
306	COM51	-4118.200	672.075
307	COM52	-4170.000	672.075
308	COM53	-4221.800	672.075
309	COM54	-4273.600	672.075
310	COM55	-4325.400	672.075
311	COM56	-4377.200	672.075
312	COM57	-4429.000	672.075
313	COM58	-4480.800	672.075
314	COM59	-4532.600	672.075
315	COM60	-4584.400	672.075
316	COM61	-4636.200	672.075
317	COM62	-4688.000	672.075
318	COM63	-4739.800	672.075
319	COM64	-4791.600	672.075
320	COM65	-4843.400	672.075
321	COM66	-4895.200	672.075
322	COM67	-4947.000	672.075
323	COM68	-4998.800	672.075
324	COM69	-5050.600	672.075
325	COM70	-5102.400	672.075
326	COM71	-5154.200	672.075
327	COM72	-5206.000	672.075
328	COM73	-5257.800	672.075
329	COM74	-5309.600	672.075
330	DUMMY	-5361.800	672.075
331	DUMMY	-5414.000	672.075



Bump size	X (um)	Y (um)
Pad 1-7,123-331	34	84
Pad 8-122	54	84

Table 2 - SSD0323Z Gold bump pad coordinates

PIN DESCRIPTION

M, DOF#
These pins are No Connection pins. Nothing should be connected to these pins, nor they are connected together. These pins should be left open individually.

CL
This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. In this case, the output clock frequency equals to the internal clock frequency. When internal oscillator is disabled, this pin receives display clock signal from external clock source.

M/S#
This pin is an input pin and must be pulled high to enable the chip function.

CLS
This pin is internal clock enable. When this pin is pulled high, internal clock is enabled.
The internal clock will be disabled when it is pulled low, an external clock source must be connected to CL pin for normal operation.

BS0, BS1, BS2
These pins are MCU interface selection input. See the following table:

Table 3 - MCU interface setting

	6800-parallel interface	8080-parallel interface	Serial interface
BS0	0	0	0
BS1	0	1	0
BS2	1	1	0

CS#
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

RES#
This pin is reset signal input. When the pin is low, initialization of the chip is executed.

D/C#
This pin is Data/Command control pin. When the pin is pulled high, the input at D_7-D_0 is treated as display data. When the pin is pulled low, the input at D_7-D_0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/W# (WR#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “LOW” for write mode. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.

E (RD#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.

D_7-D_0
These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D_1 will be the serial data input SDIN and D_0 will be the serial clock input SCLK.

V_{DD}
This is a voltage supply pin. It must be connected to external source.

V_{SS}
This is a ground pin. It also acts as a reference for the logic pins and the OLED driving voltages. It must be connected to external ground.

V_{CC}
This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC-DC voltage converter.

V_{REF}
This pin is the voltage reference for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can be either supplied externally or connected to V_{CC}.

I_{REF}
This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 10uA.

V_{COMH}
This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When V_{COMH} is generated internally, a capacitor should be connected between this pin and V_{SS}.

VSL
This pin is the output pin for the voltage output low level for SEG signals. A capacitor should be connected between this pin and V_{SS}.

VSLCAP
This pin is the output pin for the voltage output low level for SEG signals. A capacitor should be connected between this pin and V_{SS}.

VCL
This pin is the output pin for the voltage output low level for COM signals. This pin should be connected to $V_{SS.}$

VDDB
This is the power supply pin for the GDR pin buffer. It must be connected when the converter is used.

VSSB
This is the GND pin for the GDR pin buffer. It must be connected when the converter is used.

GDR
This output pin drives the gate of the external NMOS of the booster circuit.

FB
This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level(Vcc).

RESE
This pin connects to the source current pin of the external NMOS of the booster circuit.

VB_{REF}
This pin is the internal voltage reference of booster circuit. A stabilization capacitor should be connected between this pin and Vss for both internal and external VCC usage.

COM0-COM79
These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off.

SEG0-SEG127
These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off.

NC
These pins should be left open individually.

FUNCTIONAL BLOCK DESCRIPTIONS

Command Decoder
This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.
If D/C# pin is high, the input at D_7-D_0 is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D_7-D_0 is interpreted as a Command which will be decoded and be written to the corresponding command register.

MPU Parallel 6800-series Interface
The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/W#(WR#), D/C#, E (RD#), CS#. R/W#(WR#) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W# (WR#) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C# input. The E (RD#) input serves as data latch signal (clock) when high provided that CS# is low. Refer to Parallel Interface Timing Diagram of 6800-series microprocessors.
In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3 below.

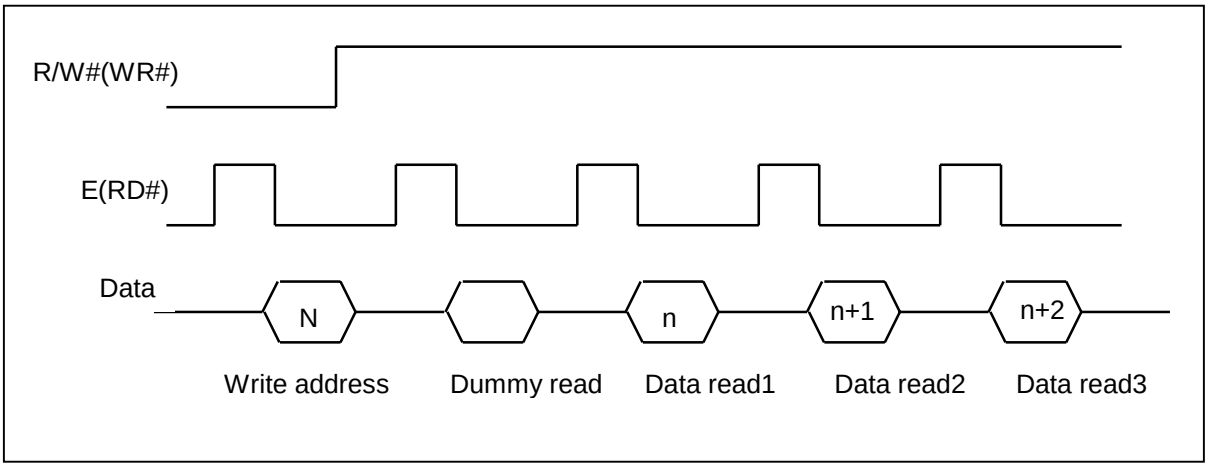


Figure 3 - Display Data Read Back Procedure - Insertion of Dummy Read

MPU Parallel 8080-series Interface
The parallel interface consists of 8 bi-directional data pins (D_7-D_0), E (RD#), R/W#(WR#), D/C#, CS#. The E (RD#) input serves as data read latch signal (clock) when it is low, and provided that CS# is low. Data read latch signal is disable when E (RD#) is high. Display data or status register read is controlled by D/C#. R/W# (WR#) input serves as data write latch signal (clock) when it is low and provided that CS# is low. Display data or command register write is controlled by D/C#. Refer to Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial Interface
The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D_7, D_6, ... D_0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

Oscillator Circuit and Display Time Generator

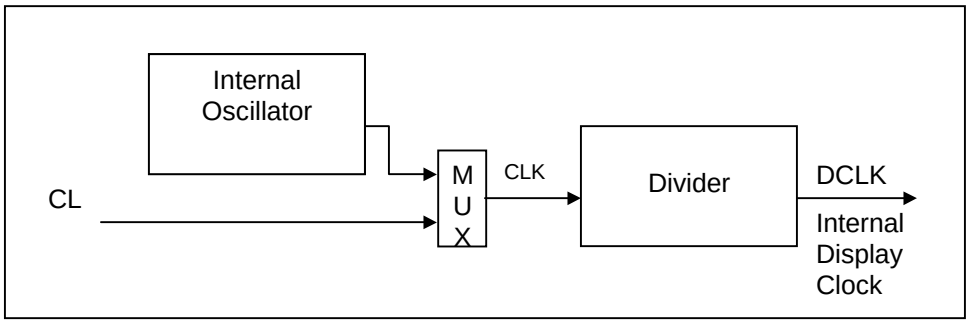


Figure 4 - Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the Display Timing Generator.

Current Control and Voltage Control

This block is used to derive the incoming power sources into the different levels of internal use voltage and current. V_{CC} and V_{DD} are external power supplies. V_{REF} is reference voltage, which is used to derive driving voltage for segments and commons. I_{REF} is a reference current source for segment current drivers.

Segment Drivers/Common Drivers

Segment drivers deliver 128 current sources to drive OLED panel. The driving current can be adjusted from 0 to 300uA with 128 steps. Common drivers generate voltage scanning pulse.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to Table 3-7 for GDDRAM address map description)

Table 4 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|									
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

Table 5 – GDDRAM address map showing Horizontal Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]	(HEX)
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
|	|										
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]	
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

Table 6 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, … , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		3F		3E			01		00		Column Address
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	(HEX)
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
|	|									
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]	
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

Table 7 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|									
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=10H)

Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, … , D5118, D5119)

Table 8 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, … , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00									
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]		
|	|								
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]		
COM79	4F									

SEG Outputs
Column Address
(HEX)

COM Outputs
(Display Startline=0)

Row Address (HEX)

Gray Scale Decoder

There are 16 gray levels from GS0 to GS15. The gray scale of the display is defined by the pulse width (PW) of current drive phase, GS0 has no pre-charge and no current drive. Each L value represents an offset to the corresponding gray scale level. See below table and graphical representation:

Table9 - Gray scale pulse width set table

	Description	Number of DCLKs
L1	Set GS1 level Pulse Width	0-7
L2	Set GS2 level Pulse Width Offset	1-8
L3	Set GS3 level Pulse Width Offset	1-8
. . .	. . .	. . .
L13	Set GS13 level Pulse Width Offset	1-8
L14	Set GS14 level Pulse Width Offset	1-8
L15	Set GS15 level Pulse Width Offset	1-8

DCLK: Internal Display Clock. It is used for defining phase clock period.

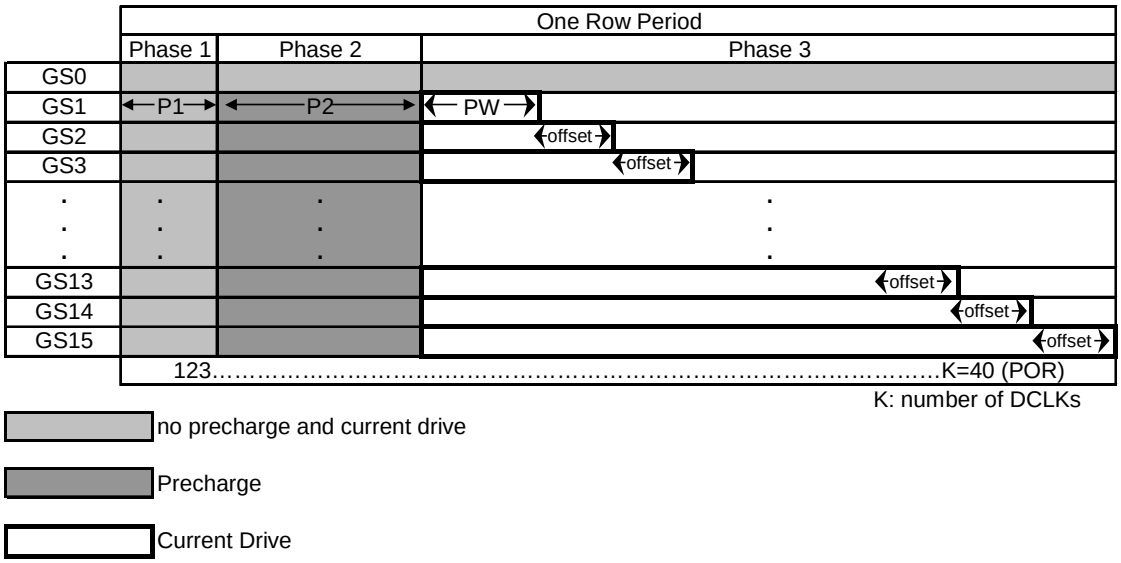


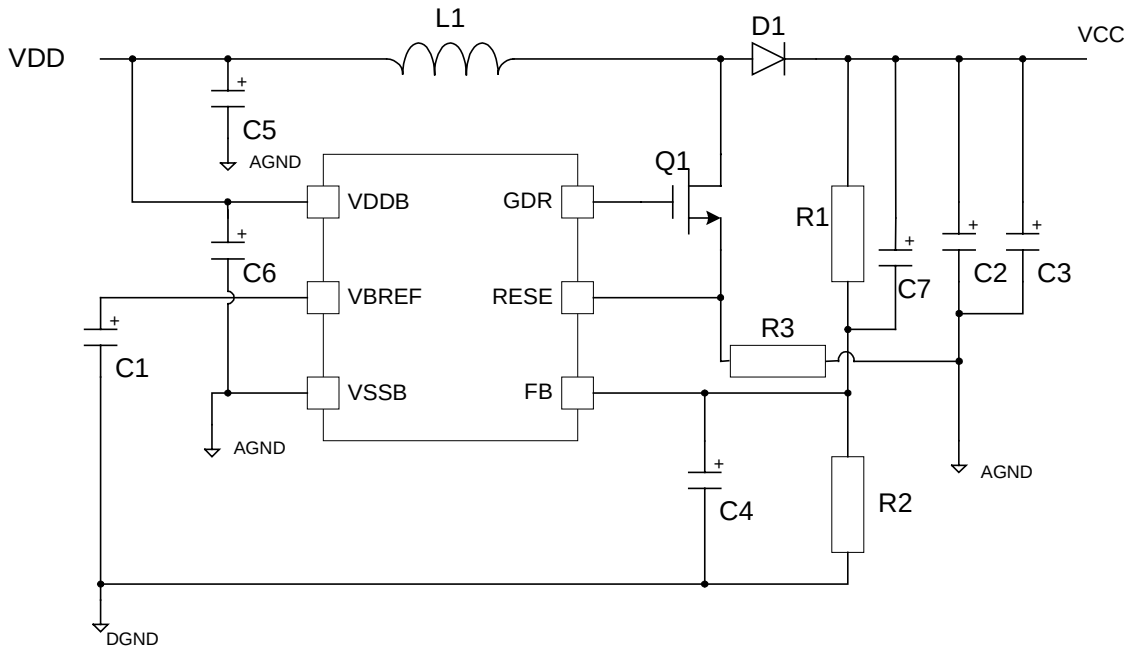
Figure 5 - Gray scale pulse width set diagram

Table 10 - Gray scale pulse width default values

POR	Result
L1=1	GS1 level Pulse width=1
L2=1	GS2 level Pulse width=3
L3=1	GS3 level Pulse width=5
L4=1	GS4 level Pulse width=7
L5=1	GS5 level Pulse width=9
L6=1	GS6 level Pulse width=11
L7=1	GS7 level Pulse width=13
L8=1	GS8 level Pulse width=15
L9=1	GS9 level Pulse width=17
L10=1	GS10 level Pulse width=19
L11=1	GS11 level Pulse width=21
L12=1	GS12 level Pulse width=23
L13=1	GS13 level Pulse width=25
L14=1	GS14 level Pulse width=27
L15=1	GS15 level Pulse width=29

DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for handheld applications. In SSD0323, internal DC-DC voltage converter accompanying with an external application circuit (shown in below figure) can generate a high voltage supply V_{CC} from a low voltage supply input V_{DD}. V_{CC} is the voltage supply to the OLED driver block. Below application circuit is an example for the input voltage of 3V VDD to generate V_{CC} of 12V @20mA ~ 30mA application.



Remark:

1. L1, D1, Q1, C5 should be grouped closed together on PCB layout.
2. R1, R2, C1, C4 should be grouped closed together on PCB layout.
3. The VCC output voltage level can be adjusted by R1and R2, the reference formula is:
   VCC = 1.2 x (R1+R2) / R2
   The value of (R1+R2) should be between 500k to 1M Ohm.

Table 11 - Passive component selection:

Components	Typical Value	Remark
L1	Inductor, 22µH	2A
D1	Schottky diode	2A, 25V e.g. 1N5822
Q1	MOSFET	N-FET with low R_{DS}(on) and low Vth voltage. e.g. MGSF1N02LT1 [ON SEMICONDUCTOR]
R1, R2	Resistor	1%,1/10W
R3	Resistor, 1.5Ω	1%, 1/2W
C1	Capacitor, 1µF	16V
C2	Capacitor, 22µF	Low ESR, 25V
C3	Capacitor, 1µF	16V
C4	Capacitor, 10nF	16V
C5	Capacitor, 1 ~ 10 µF	16V
C6	Capacitor, 0.1 ~ 1µF	16V
C7	Capacitor, 15nF	16V

COMMAND TABLE

Table 12 - Command Table

(D/C# =0, R/W#(WR#)=0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	15	0	0	0	1	0	1	0	1	Set Column Address	Second command A[5:0] sets the column start address from 0-63, POR = 00H.
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		Third command B[5:0] sets the column end address from 0-63, POR = 3FH.
0	75	0	1	1	1	0	1	0	1	Set Row address	Second command A[6:0]sets the row start address from 0-79, POR = 00H.
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		Third command B[6:0] sets the row end address from 0-79, POR = 4FH.
0	81	1	0	0	0	0	0	0	1	Set Contrast Control Register	Double byte command to select 1 out of 128 contrast steps. Contrast increases as level increase. The level is set to 40H after POR
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	84~86	1	0	0	0	0	1	X_1	X_0	Set Current Range	84H = Quarter Current Range (POR) 85H = Half Current Range 86H = Full Current Range
0	A0	1	0	1	0	0	0	0	0	Set Re-map	A[0]=0, Disable Column Address Re-map (POR)
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[0]=1, Enable Column Address Re-map A[1]=0, Disable Nibble Re-map (POR) A[1]=1, Enable Nibble Re-map A[2]=0, Horizontal Address Increment (POR) A[2]=1, Vertical Address Increment A[4]=0, Disable COM Re-map disable (POR) A[4]=1, Enable COM Re-map A[5]=0, Reserved (POR) A[5]=1, Reserved A[6]=0, Disable COM Split Odd Even (POR) A[6]=1, Enable COM Split Odd Even
0	A1	1	0	1	0	0	0	0	1	Set Display Start Line	Set display RAM display start line register from 0-79.
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Display start line register is reset to 00H after POR.
0	A2	1	0	1	0	0	0	1	0	Set Display Offset	Set vertical scroll by COM from 0-79.
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		The value is reset to 00H after POR.
0	A4~A7	1	0	1	0	0	X_2	X_1	X_0	Set Display Mode	A4H = Normal Display (POR) A5H = Entire Display On, all pixels turns on in GS level 15 A6H = Entire Display Off, all pixels turns off A7H = Inverse Display

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	A8 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX, POR=4FH(80MUX)
0 0	AD A[1:0]	1 *	0 *	1 *	0 *	1 *	1 *	0 A_1	1 A_0	Set Master Configuration	A[0] = 0, Disable DC-DC converter A[0] = 1, Enable DC-DC converter (POR) A[1] = 0, Disable internal VCOMH A[1] = 1, Enable internal VCOMH (POR)
0	AE~AF	1	0	1	0	X_3	1	1	1	Set Display On/Off	AEH = Display Off (Sleep mode) (POR) AFH = Display On
0 0	B0 A[5:0]	1 *	0 *	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Pre-charge Compensation Enable	A[5:0] = 08h (POR) A[5:0] = 28h, Enable pre-charge compensation
0 0	B4 A[2:0]	1 *	0 *	1 *	1 *	0 *	1 A_2	0 A_1	0 A_0	Set Pre-charge Compensation Level	A[2:0] = 0 (POR) A[2:0] = 3h, Recommended level
0 0	BF A[3:0]	1 *	0 *	1 *	1 *	1 A_3	1 A_2	1 A_1	1 A_0	Set Segment Low Voltage(VSL)	Second command A[3:0] sets the VSL voltage as follow: 1000-1110 A[3:0] = 0010 connects to VSS A[3:0] = 1110 (POR) (When VDD > 2.5V)
0 0	BE A[5:0]	1 *	0 *	1 A_5	1 A_4	1 A_3	1 A_2	1 A_1	0 A_0	Set VCOMH Voltage	Second command A[5:0] sets the VCOMH voltage level 000000-011111 A[5:0] = 1xxxxx = 1.0*VREF A[5:0] = 010001(POR)
0 0	BC A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	1 A_3	1 A_2	0 A_1	0 A_0	Set Precharge Voltage	Second command A[7:0] sets the precharge voltage level 00000000-00011111 A[7:0] = 1xxxxxxx connects to VCOMH A[7:0] = 001xxxxx equals 1.0*VREF A[7:0] = 00011000(POR)
0 0 0	B1 A[3:0] A[7:4]	1 * A_7	0 * A_6	1 * A_5	1 * A_4	0 A_3 *	0 A_2 *	0 A_1 *	1 A_0 *	Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLK clocks, POR = 3DLKS = 3H A[7:4] = P2, phase 2 period of 1-15 DCLK clocks, POR = 5DLKS = 5H
0 0	B2 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Row Period	The next command sets the number of DCLKs, K, per row between 2-158DLKS, POR = 37DLKS = 25H The K value should be set as K = P1+P2+GS15 pulse width (POR: 3+5+29DLKS)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B3	1	0	1	1	0	0	1	1	Set Display Clock Divide Ratio/Oscillator Frequency	The lower nibble of the next command sets the divide ratio of the display clocks:
0	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	A[7:4]	A_7	A_6	A_5	A_4	*	*	*	*		Divide ratio = 1-16, POR = 2
											The higher nibble of the next command sets the Oscillator Frequency. Oscillator Frequency increases with the value of
											A[7:4] and vice versa. POR=0
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next eight bytes of command set the gray scale level of GS1-15 as below:
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		A[2:0] = L1, POR=1
0	B[6:4]	*	B_6	B_5	B_4	*	*	*	*		B[2:0] = L2, POR=1
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		B[6:4] = L3, POR=1
0	C[6:4]	*	C_6	C_5	C_4	*	*	*	*		C[2:0] = L4 POR=1
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		C[6:4] = L5, POR=1
0	D[6:4]	*	D_6	D_5	D_4	*	*	*	*		D[2:0] = L6, POR=1
0	E[2:0]	*	*	*	*	*	E_2	E_1	E_0		D[6:4] = L7, POR=1
0	E[6:4]	*	E_6	E_5	E_4	*	*	*	*		E[2:0] = L8, POR=1
0	F[2:0]	*	*	*	*	*	F_2	F_1	F_0		E[6:4] = L9, POR=1
0	F[6:4]	*	F_6	F_5	F_4	*	*	*	*		F[2:0] = L10, POR=1
0	G[2:0]	*	*	*	*	*	G_2	G_1	G_0		F[6:4] = L11, POR=1
0	G[6:4]	*	G_6	G_5	G_4	*	*	*	*		G[2:0] = L12, POR=1
0	H[2:0]	*	*	*	*	*	H_2	H_1	H_0		G[6:4] = L13, POR=1
0	H[6:4]	*	H_6	H_5	H_4	*	*	*	*		H[2:0] = L14, POR=1
											H[6:4] = L15, POR=1
0	CF	1	1	0	0	1	1	1	1	Set Biasing Current for DC-DC converter	F0H = High (POR)
0	A[7:6]	A_7	A_6	*	*	*	*	*	*		70H = Low
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Table 13 - Read Command Table

(D/C#=0, R/W#(WR#)=1, E(RD#)=1 for 6800 or E(RD#)=0 for 8080)

$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D7 = 0:reserved D7 = 1:reserved D6 = 0:indicates the display is ON D6 = 1:indicated the display is OFF D5 = 0:reserved D5 = 1:reserved D4 = 0:reserved D4 = 1:reserved

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command;
Otherwise, unexpected result will occur

Data Read / Write

To read data from the GDDRAM, input High to R/W# (WR#) pin and D/C# pin for 6800-series parallel mode, Low to E (RD#) pin and High to D/C# pin for 8080-series parallel mode.

In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data read. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/W#(WR#) pin and High to D/C# pin for 6800-series parallel mode and 8080-series parallel mode. For serial interface mode, it is always in write mode. In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data write. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data write.

It should be noted that, in horizontal address increment mode, the row address pointer would be increased by one automatically if the column address pointer wraps around. In vertical address increment mode, the column address pointer will be increased by one automatically if the row address pointer wraps around.

Table 14 - Address Increment Table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

COMMAND DESCRIPTIONS

Set Column Address

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address.

Set Row Address

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address.

Set Contrast Control Register

This command is to set Contrast Setting of the display. The chip has 128 contrast steps from 00H to 7FH. The segment output current increases linearly with the increase of contrast step. See Figure 6 below.

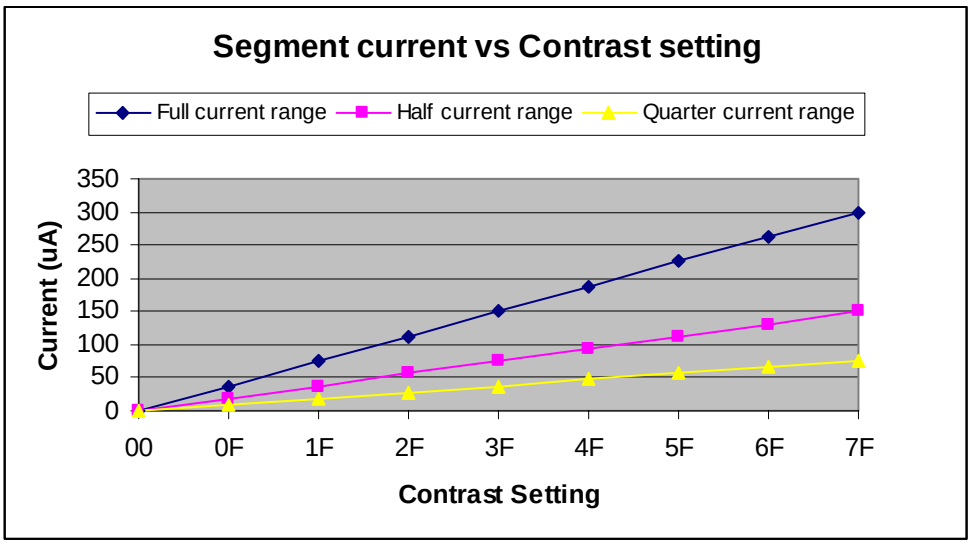


Figure 6 - Segment current vs Contrast setting

Set Current Range

This command is used to select quarter range or half range or full range current mode. With the same contrast level, quarter range mode will give a quarter of the current output of the full range mode. Similar to half range current mode, it will give a half of the current output of the full range mode. See Figure 6. In POR, quarter range current mode is default.

Set Re-map

This command changes the mapping between the display data column address and segment driver, row address and common driver. It allows flexibility in layout during OLED module assembly. See the Re-map setting below:

Column Address Re-map

If column address re-map is set, Col 0-63 map to SEG127-0, regardless of start column and end column commands.

Nibble Re-map

If nibble re-map is set, the two nibbles of the data bus for RAM access are re-mapped, such that (D7, D6, D5, D4, D3, D2, D1, D0) acts like (D3, D2, D1, D0, D7, D6, D5, D4)

This feature working with Column Address Re-map would produce an effect of flipping outputs SEG0-127 to SEG127-SEG0.

Address Increment Mode
If horizontal increment mode is set, the column address pointer advances after each RAM access.
If vertical increment mode is set, the row address pointer advances after each RAM access.

COM Re-map
If COM re-map is set, ROW 0-79 map to COM79-0, regardless of start and end row commands.

Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 79.

Set Display Offset

This is a double byte command. The next command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-79.
For example, to move the COMX towards the COM0 direction for L lines, the 7-bit data in the second command should be given by L. In other words, to move the COMX towards the COM79 direction for L lines, the 7-bit data in the second command should be given by 80-L.

Set Display Mode

This command is used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display. Set Entire Display On forces the entire display to be at gray level “GS15” regardless of the contents of the display data RAM. Set Entire Display Off forces the entire display to be at gray level “GS0” regardless of the contents of the display data RAM. Normal Display will turn the data to ON at the corresponding gray level. Inverse display will turn the data as follow:

Table 15 - Mapping of data with each gray scale level at different display mode

Data $D_{X4}D_{X3}D_{X2}D_{X1}$	Normal Display (A4H)	Entire Display On (A5H)	Entire Display Off (A6H)	Inverse Display (A7H)
0000	GS0	GS15	GS0	GS15
0001	GS1	GS15	GS0	GS14
0010	GS2	GS15	GS0	GS13
0011	GS3	GS15	GS0	GS12
0100	GS4	GS15	GS0	GS11
0101	GS5	GS15	GS0	GS10
0110	GS6	GS15	GS0	GS9
0111	GS7	GS15	GS0	GS8
1000	GS8	GS15	GS0	GS7
1001	GS9	GS15	GS0	GS6
1010	GS10	GS15	GS0	GS5
1011	GS11	GS15	GS0	GS4
1100	GS12	GS15	GS0	GS3
1101	GS13	GS15	GS0	GS2
1110	GS14	GS15	GS0	GS1
1111	GS15	GS15	GS0	GS0

Set Multiplex Ratio

This command sets multiplex ratio from 16 to 80. In POR, multiplex ratio is 80.

Set DC-DC Converter

This command is used to enable or disable the internal DC-DC voltage converter. This command will be executed when display is on.

Set Display On/Off

This command turns the display on or off. When the display is off, the segment and common output are in high impedance state.

Set Segment Low voltage

This command is used to set segment low voltage (VSL). The value of VSL is the same for display all on, display all off pattern with either internal or external DC-DC voltage converter.

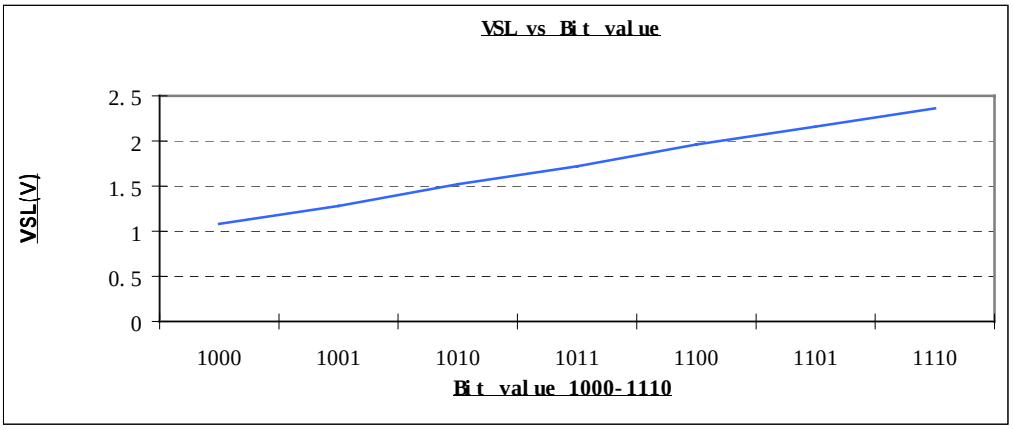


Figure 7 - VSL vs Bit value

Set V_{COMH} Voltage

This command is used to set V_{COMH} voltage level

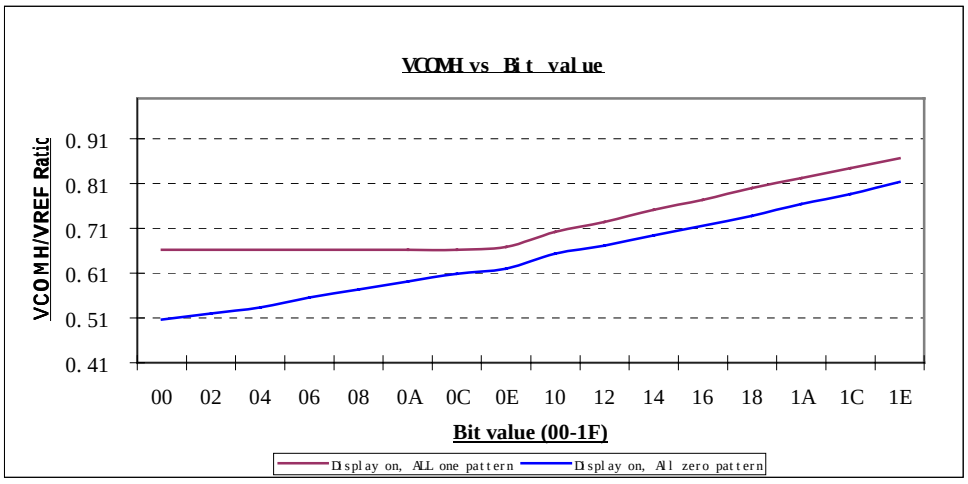


Figure 8 - VCOMH vs Bit value

Set Precharge Voltage

This command is used to set Precharge Voltage level

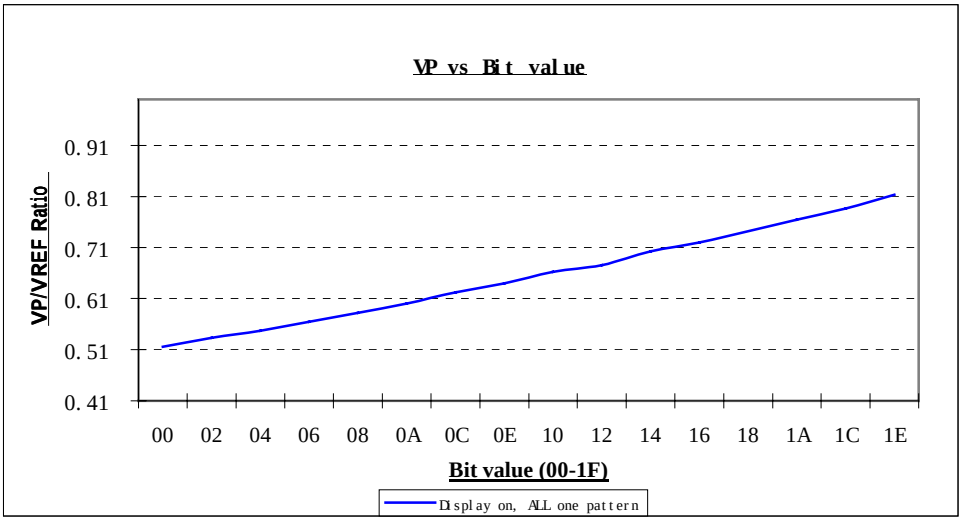


Figure 9 - VP vs Bit value

Set Phase Length

This is a double byte command. The lower nibble of the second byte selects phase 1 period (no pre-charge and current drive) from 1 to 16 DCLKs. POR is A[3:0]=3d. The higher nibble of the second byte is used to select phase 2 period (pre-charge) from 1 to 16 DCLKs. POR is A[7:4]=5d.

Set Row Period

This command is used to set the row period. It is defined by multiplying the internal display clock period by the number of internal display clocks per row (Value from 2-158d). POR is 37d. The larger the value, the more precise of each gray scale level can be tuned. See “Gray Scale Table” command for details. Also, It is used to define the frame frequency with the use of “Display Clock Divide Ratio” command together.

Row period equals to the sum of phase 1, 2 periods and the pulse width of GS15. See equation in command table on page 12.

Set Display Clock Divide Ratio

This command is used to set the frequency of the internal display clocks, DCLKs. It is defined by dividing the oscillator frequency by the divide ratio (Value from 1 to 16). POR is 2. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency. See equation on page 12.

Set Oscillator Frequency

This is a double byte command. The lower nibble of the second byte is used to select the oscillator frequency. Default value is shown in Table 12.

Set Gray Scale Table

This command is used to set the gray scale table for the display. Except GS0, which has no pre-charge and current drive, each GS level is programmed by a set of offset values. As shown in Table 8, GS1 is defined with pulse width equals to the first offset value, L1, select from 0-7 internal display clocks. GS2 is defined with pulse width equals to GS1 plus the next offset value, L2, select from1-8 internal display clocks. Similarly, the next GS level is defined with pulse width equals to its lower one GS level plus the next offset value, select from 1-8 internal display clocks. In normal operation, GS15 should take the full current drive period as its pulse width. Therefore, the row period should be set as the sum of phase 1 period, phase 2 period, and the pulse width of GS15 with the use of “Row period” command.

NOP

No Operation Command.

Status register Read

This command is issued by setting D/C# low during a data read (refer to Figure 10 and Figure 11 parallel interface waveform). It allows the MCU to monitor the internal status of the chip.

MAXIMUM RATINGS

Table 16 - Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 16	V
V_{REF}		0 to 16	V
V_{COMH}	Supply Voltage/Output voltage	0 to 16	V
-	SEG/COM output voltage	0 to 16	V
V_{in}	Input voltage	Vss-0.3 to Vdd+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

DC CHARACTERISTICS

Table 17 - DC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	8	12	16	V
V_{DD}	Logic Supply Voltage	-	2.4	2.7	3.5	V
V_{OH}	High Logic Output Level	IOUT = 100uA, 3.3MHz	0.9*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	IOUT = 100uA, 3.3MHz	0	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	IOUT = 100uA, 3.3MHz	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	IOUT = 100uA, 3.3MHz	0	-	0.2*V_{DD}	V
I_{SLEEP}	Sleep mode Current	No loading	-	0.2	5	uA
I_{CC}	V_{CC} Supply Current VDD=2.7V, external VCC=12V, IREF=10uA, Frame rate=110Hz, All one pattern, Display on, no loading	Contrast = 7F	-	700	-	uA
I_{DD}	V_{DD} Supply Current VDD=2.7V, external VCC=12V, IREF=10uA, Frame rate=110Hz, All one pattern, Display on, no loading	Contrast = 7F	-	-	650	uA
I_{SEG}	Segment Output Current VDD=2.7V, VCC=12V, IREF=10uA, Frame rate=110Hz, Display on, Segment pin under test is connected with a 20K resistive load to VSS	Contrast = 7F	270	300	370	uA
		Contrast = 5F	-	225	-	
		Contrast = 3F	-	150	-	
		Contrast = 1F	-	75	-	
Dev	Segment output current uniformity V_{DD}=2.7V, V_{CC}=12V, I_{REF}=10uA, Contrast=7F	Adjacent pin	-	±2	-	%
		Overall pin to pin	-	-	±3	
Vcc	DC-DC converter output voltage	VDD input=3V, L=22uH; R1=450Kohm; R2=50Kohm; Icc = 20mA(loading)	10	-	12	V
Pwr	DC-DC converter output power	VDD input=3V, L=22uH; Vcc = 12V	-	-	400	mW

AC CHARACTERISTICS

Table 18 - AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	Vdd = 2.7V	535	630	725	kHz
F_{FRM}	Frame Frequency for 128 MUX Mode	128x80 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} X 1/(D*K*80)	-	Hz

D: divide ratio
K: number of display clocks
Refer to command table for detail description

Table 19 - 6800-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

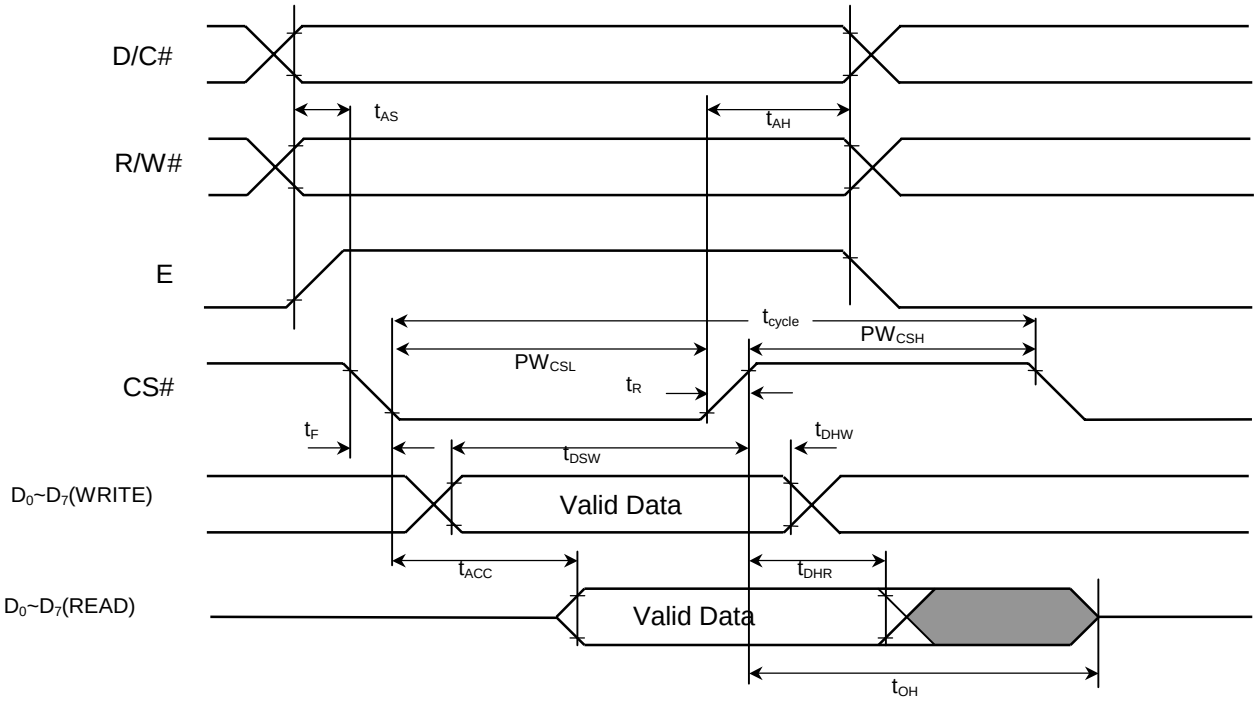


Figure 10 - 6800-series MPU Parallel Interface Characteristics

Table 20 - 8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

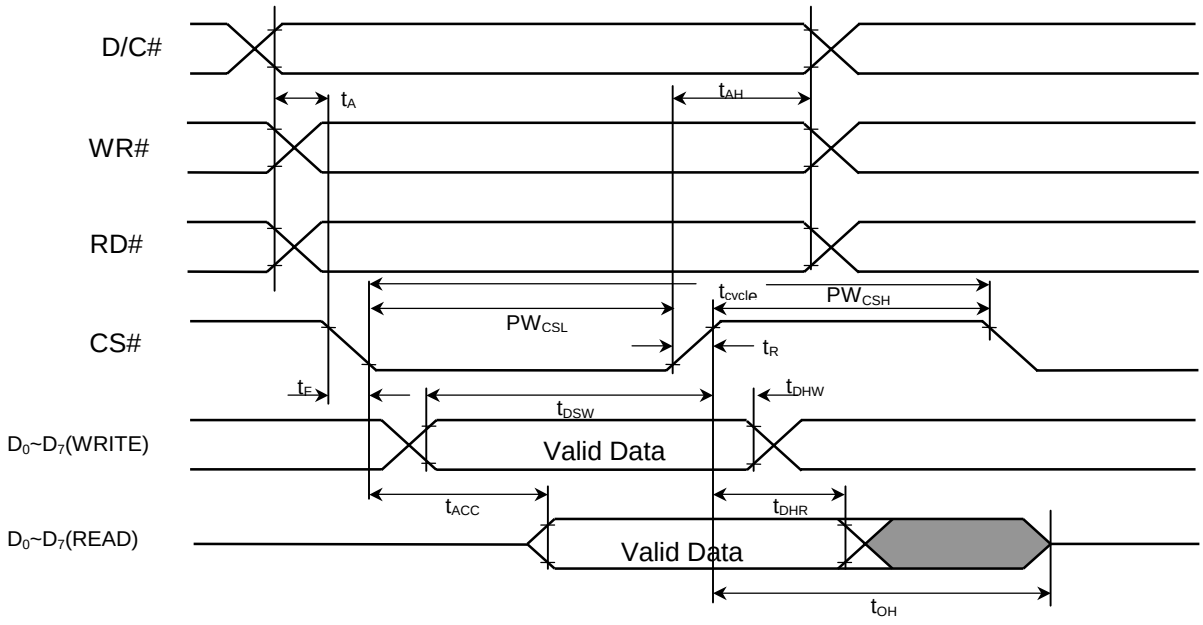


Figure 11 - 8080-series MPU Parallel Interface Characteristics

Table 21 - Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

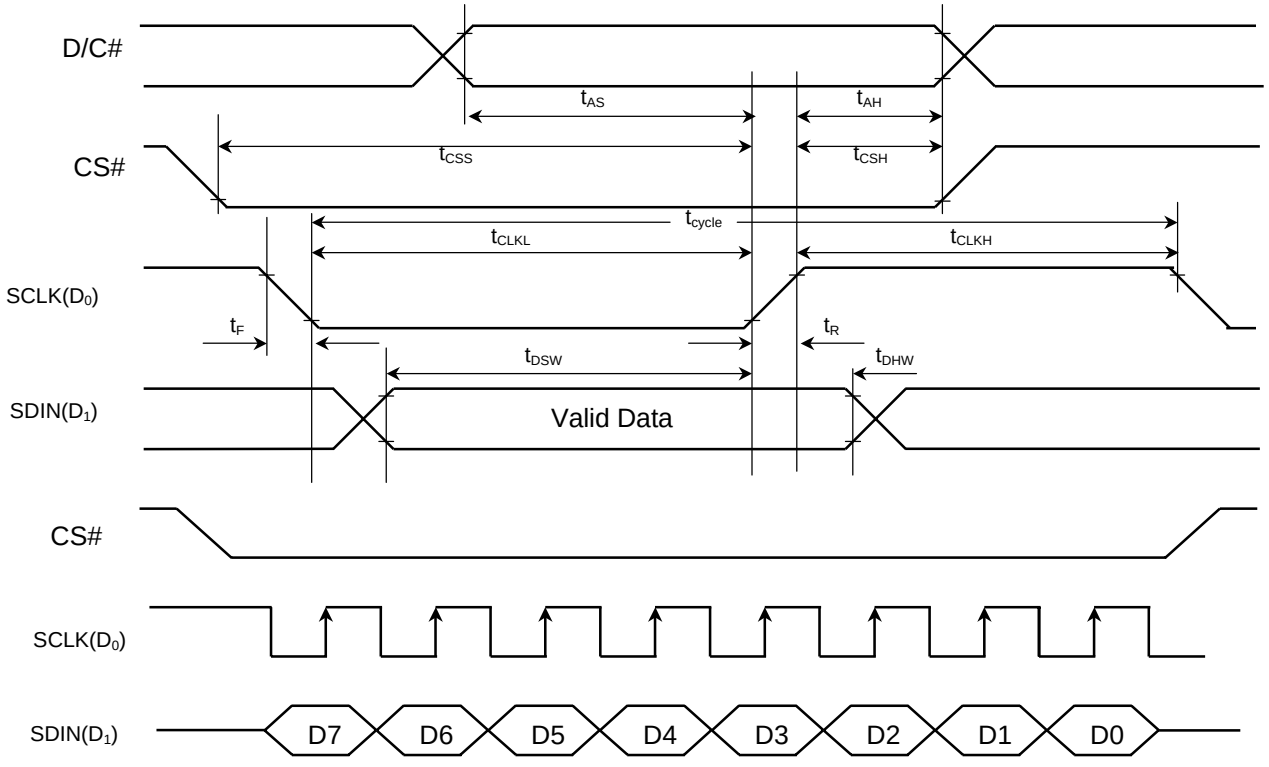


Figure 12 - Serial Interface Characteristics

SSD0323Z DIE TRAY DIMENSIONS

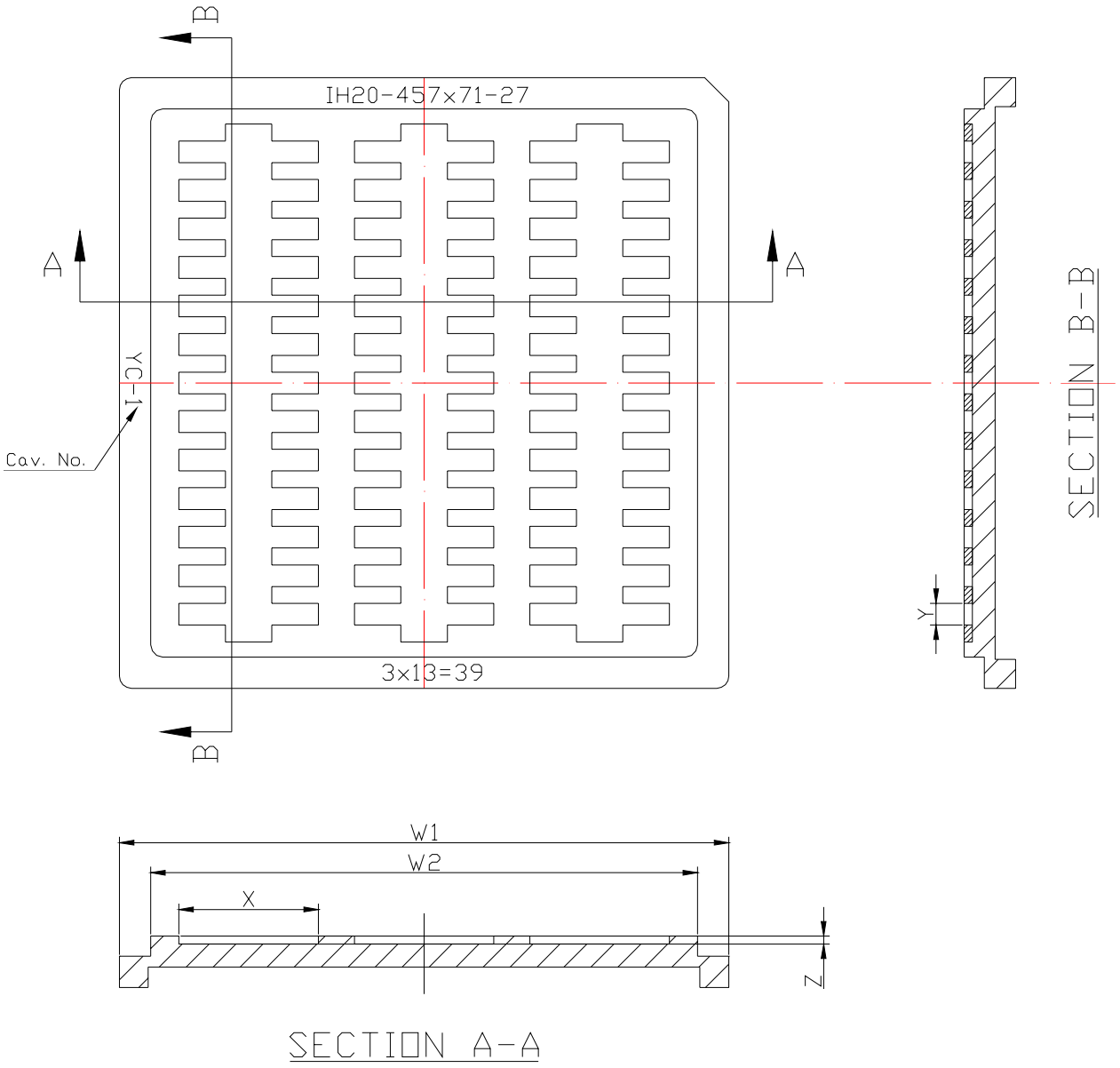


Figure 13 - SSD0323Z Die Tray Drawing

Table 22 - SSD0323Z Die Tray Dimensions

Parameter	Dimensions
W1	50.70±0.2 mm
W2	45.50±0.2 mm
X	11.60±0.1 mm
Y	1.80±0.1 mm
Z	0.71±0.05 mm
N (number of die)	39

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