SSD0332

Advance Information

96RGB x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

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TABLES

FIGURES

1 GENERAL DESCRIPTION

The SSD0332 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 288 segments (96RGB) and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD0332 displays data directly from its internal 96x64x16 bits Graphic Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable I^2C Interface, 6800/8000 series compatible Parallel Interface or Serial Peripheral Interface. It has a 256 steps contrast control and 65K color control.

2 FEATURES

- Support max. 96RGB x 64 matrix panel
- Power supply: V_{DD} = 2.4V - 3.5V
  V_{CC} = 7.0V - 18.0V
- OLED driving output voltage, 16V maximum
- DC-DC voltage converter
- Segment maximum source current: 200uA
- Common maximum sink current: 50mA
- Embedded 96x64x16 bit SRAM display buffer
- 16 step master current control, and 256 step current control for the three color components
- Programmable Frame Rate
- Graphic Acceleration Command Set (GAC)
- I^2C Interface, 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature: -40 to 90 °C

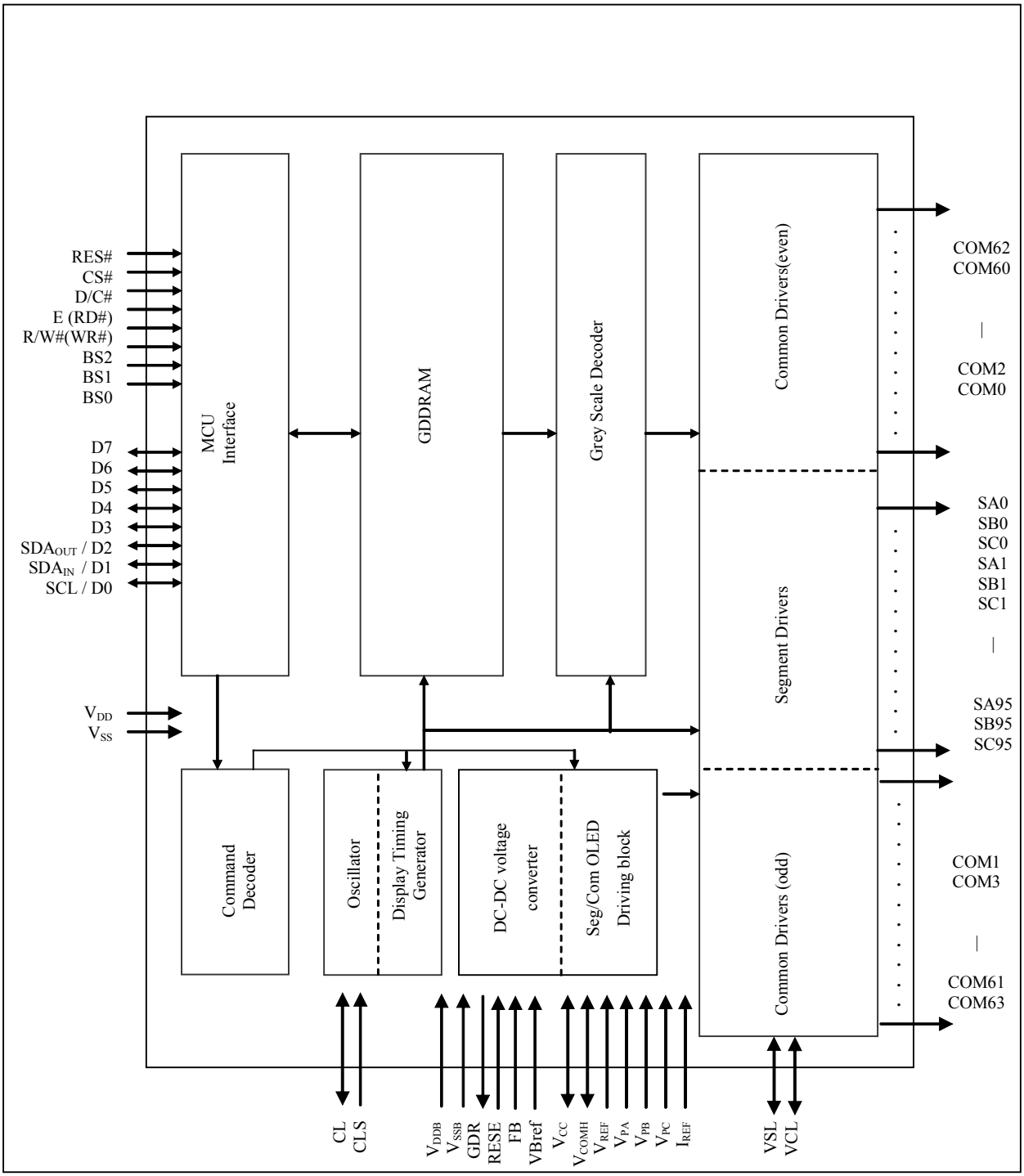
3 ORDERING INFORMATION

Table 3-1: Ordering Information

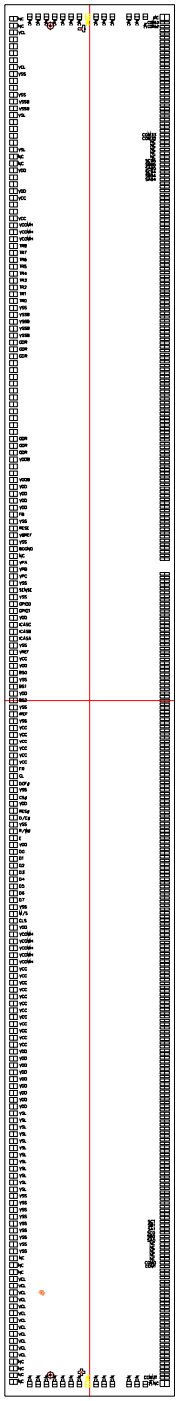
Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD0332Z	96RGB	64	COG	Page 8	• Min SEG pad pitch: 41.2 um • Min COM pad pitch: 41.2 um

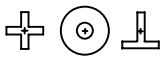
4 BLOCK DIAGRAM

Figure 4-1 : SSD0332 Block Diagram



Pad #1





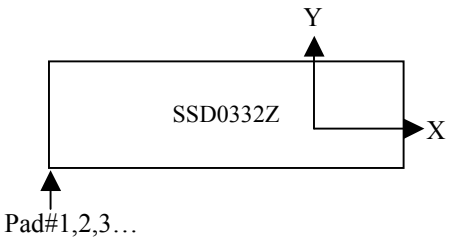
\+ represents the centre of the alignment mark

	X-pos (um)	Y-pos (um)
	-7433.6	-90.5
	7433.6	-90.5
	-7465.9	-437.4
	7465.9	-437.4

All alignment keys have size 75 um x 75 um

Die Size: 15.4mm x 1.9mm
Die Thickness: 457 +/- 25 um
Min I/O pad pitch: 76.2 um
Min SEG pad pitch: 41.2 um
Min COM pad pitch: 41.2 um
Bump Height: Nominal 15 um

Bump size / Pad #	X-Dimension	Y-Dimension
1 - 199	54.000um	84.000um
200 ~ 213, 578 ~ 591	50.000um	60.000um
215 ~ 576	27.000um	110.000um
214, 577	68.200um	110.000um



Gold Bumps face up

Table 5-1 : SSD0332Z Die Pad Coordinates

Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis
1	NC	-7543.80	-853.00	81	VPB	-1447.80	-853.00	161	VSL	4648.20	-853.00	241	COM5	6427.20	840.00
2	NC	-7467.60	-853.00	82	VPC	-1371.60	-853.00	162	VSL	4724.40	-853.00	242	COM4	6386.00	840.00
3	VCL	-7391.40	-853.00	83	VSS	-1295.40	-853.00	163	VSL	4800.60	-853.00	243	COM3	6344.80	840.00
4	VCL	-7315.20	-853.00	84	SENSE	-1219.20	-853.00	164	VSL	4876.80	-853.00	244	COM2	6303.60	840.00
5	VCL	-7239.00	-853.00	85	VSS	-1143.00	-853.00	165	VSL	4953.00	-853.00	245	COM1	6262.40	840.00
6	VCL	-7162.80	-853.00	86	GPIO0	-1066.80	-853.00	166	VSL	5029.20	-853.00	246	COM0	6221.20	840.00
7	VCL	-7086.60	-853.00	87	GPIO1	-990.60	-853.00	167	VSL	5105.40	-853.00	247	NC	6180.00	840.00
8	VCL	-7010.40	-853.00	88	VDD	-914.40	-853.00	168	VSL	5181.60	-853.00	248	NC	6138.80	840.00
9	VSS	-6934.20	-853.00	89	ICASC	-838.20	-853.00	169	VSL	5257.80	-853.00	249	NC	6097.60	840.00
10	VSS	-6858.00	-853.00	90	ICASB	-762.00	-853.00	170	VSL	5334.00	-853.00	250	NC	6056.40	840.00
11	VSS	-6781.80	-853.00	91	ICASA	-685.80	-853.00	171	VSL	5410.20	-853.00	251	NC	6015.20	840.00
12	VSS	-6705.60	-853.00	92	VSS	-609.60	-853.00	172	VSS	5486.40	-853.00	252	SA0	5974.00	840.00
13	VSSB	-6629.40	-853.00	93	VREF	-533.40	-853.00	173	VSS	5562.60	-853.00	253	SB0	5932.80	840.00
14	VSSB	-6553.20	-853.00	94	VCC	-457.20	-853.00	174	VSS	5638.80	-853.00	254	SC0	5891.60	840.00
15	VSL	-6477.00	-853.00	95	VDD	-381.00	-853.00	175	VSS	5715.00	-853.00	255	SA1	5850.40	840.00
16	VSL	-6400.80	-853.00	96	BS0	-304.80	-853.00	176	VSS	5791.20	-853.00	256	SB1	5809.20	840.00
17	VSL	-6324.60	-853.00	97	VSS	-228.60	-853.00	177	VSS	5867.40	-853.00	257	SC1	5768.00	840.00
18	VSL	-6248.40	-853.00	98	BS1	-152.40	-853.00	178	VSS	5943.60	-853.00	258	SA2	5726.80	840.00
19	VSL	-6172.20	-853.00	99	VDD	-76.20	-853.00	179	VSS	6019.80	-853.00	259	SB2	5685.60	840.00
20	VSL	-6096.00	-853.00	100	BS2	0.00	-853.00	180	VSS	6096.00	-853.00	260	SC2	5644.40	840.00
21	NC	-6019.80	-853.00	101	VSS	76.20	-853.00	181	NC	6172.20	-853.00	261	SA3	5603.20	840.00
22	NC	-5943.60	-853.00	102	IREF	152.40	-853.00	182	NC	6248.40	-853.00	262	SB3	5562.00	840.00
23	VDD	-5867.40	-853.00	103	VSS	228.60	-853.00	183	NC	6324.60	-853.00	263	SC3	5520.80	840.00
24	VDD	-5791.20	-853.00	104	VCC	304.80	-853.00	184	VCL	6400.80	-853.00	264	SA4	5479.60	840.00
25	VDD	-5715.00	-853.00	105	VCC	381.00	-853.00	185	VCL	6477.00	-853.00	265	SB4	5438.40	840.00
26	VDD	-5638.80	-853.00	106	VCC	457.20	-853.00	186	VCL	6553.20	-853.00	266	SC4	5397.20	840.00
27	VCC	-5562.60	-853.00	107	VCC	533.40	-853.00	187	VCL	6629.40	-853.00	267	SA5	5356.00	840.00
28	VCC	-5486.40	-853.00	108	VCC	609.60	-853.00	188	VCL	6705.60	-853.00	268	SB5	5314.80	840.00
29	VCC	-5410.20	-853.00	109	VCC	685.80	-853.00	189	VCL	6781.80	-853.00	269	SC5	5273.60	840.00
30	VCC	-5334.00	-853.00	110	FR	762.00	-853.00	190	VCL	6858.00	-853.00	270	SA6	5232.40	840.00
31	VCOMH	-5257.80	-853.00	111	CL	838.20	-853.00	191	VCL	6934.20	-853.00	271	SB6	5191.20	840.00
32	VCOMH	-5181.60	-853.00	112	DOF#	914.40	-853.00	192	VCL	7010.40	-853.00	272	SC6	5150.00	840.00
33	VCOMH	-5105.40	-853.00	113	VSS	990.60	-853.00	193	VCL	7086.60	-853.00	273	SA7	5108.80	840.00
34	TR8	-5029.20	-853.00	114	CS#	1066.80	-853.00	194	VCL	7162.80	-853.00	274	SB7	5067.60	840.00
35	TR7	-4953.00	-853.00	115	VDD	1143.00	-853.00	195	VCL	7239.00	-853.00	275	SC7	5026.40	840.00
36	TR6	-4876.80	-853.00	116	RES#	1219.20	-853.00	196	NC	7315.20	-853.00	276	SA8	4985.20	840.00
37	TR5	-4800.60	-853.00	117	D/C#	1295.40	-853.00	197	NC	7391.40	-853.00	277	SB8	4944.00	840.00
38	TR4	-4724.40	-853.00	118	VSS	1371.60	-853.00	198	NC	7467.60	-853.00	278	SC8	4902.80	840.00
39	TR3	-4648.20	-853.00	119	R/W#	1447.80	-853.00	199	NC	7543.80	-853.00	279	SA9	4861.60	840.00
40	TR2	-4572.00	-853.00	120	E/RD#	1524.00	-853.00	200	NC	7568.30	-664.83	280	SB9	4820.40	840.00
41	TR1	-4495.80	-853.00	121	VDD	1600.20	-853.00	201	NC	7568.30	-572.83	281	SC9	4779.20	840.00
42	TR0	-4419.60	-853.00	122	D0	1676.40	-853.00	202	NC	7568.30	-480.83	282	SA10	4738.00	840.00
43	VSS	-4343.40	-853.00	123	D1	1752.60	-853.00	203	NC	7568.30	-388.83	283	SB10	4696.80	840.00
44	VSSB	-4267.20	-853.00	124	D2	1828.80	-853.00	204	NC	7568.30	-296.83	284	SC10	4655.60	840.00
45	VSSB	-4191.00	-853.00	125	D3	1905.00	-853.00	205	NC	7568.30	-204.83	285	SA11	4614.40	840.00
46	VSSB	-4114.80	-853.00	126	D4	1981.20	-853.00	206	NC	7568.30	-112.83	286	SB11	4573.20	840.00
47	VSSB	-4038.60	-853.00	127	D5	2057.40	-853.00	207	NC	7568.30	-20.83	287	SC11	4532.00	840.00
48	GDR	-3962.40	-853.00	128	D6	2133.60	-853.00	208	NC	7568.30	71.18	288	SA12	4490.80	840.00
49	GDR	-3886.20	-853.00	129	D7	2209.80	-853.00	209	NC	7568.30	163.18	289	SB12	4449.60	840.00
50	GDR	-3810.00	-853.00	130	VSS	2286.00	-853.00	210	NC	7568.30	255.18	290	SC12	4408.40	840.00
51	GDR	-3733.80	-853.00	131	M/S	2362.20	-853.00	211	NC	7568.30	439.18	291	SA13	4367.20	840.00
52	GDR	-3657.60	-853.00	132	CLS	2438.40	-853.00	212	NC	7568.30	531.18	292	SB13	4326.00	840.00
53	GDR	-3581.40	-853.00	133	VDD	2514.60	-853.00	213	NC	7568.30	623.18	293	SC13	4284.80	840.00
54	GDR	-3505.20	-853.00	134	VCOMH	2590.80	-853.00	214	NC	7560.20	840.00	294	SA14	4243.60	840.00
55	GDR	-3429.00	-853.00	135	VCOMH	2667.00	-853.00	215	COM31	7498.40	840.00	295	SB14	4202.40	840.00
56	GDR	-3352.80	-853.00	136	VCOMH	2743.20	-853.00	216	COM30	7457.20	840.00	296	SC14	4161.20	840.00
57	GDR	-3276.60	-853.00	137	VCOMH	2819.40	-853.00	217	COM29	7416.00	840.00	297	SA15	4120.00	840.00
58	GDR	-3200.40	-853.00	138	VCOMH	2895.60	-853.00	218	COM28	7374.80	840.00	298	SB15	4078.80	840.00
59	GDR	-3124.20	-853.00	139	VCC	2971.80	-853.00	219	COM27	7333.60	840.00	299	SC15	4037.60	840.00
60	GDR	-3048.00	-853.00	140	VCC	3048.00	-853.00	220	COM26	7292.40	840.00	300	SA16	3996.40	840.00
61	GDR	-2971.80	-853.00	141	VCC	3124.20	-853.00	221	COM25	7251.20	840.00	301	SB16	3955.20	840.00
62	GDR	-2895.60	-853.00	142	VCC	3200.40	-853.00	222	COM24	7210.00	840.00	302	SC16	3914.00	840.00
63	GDR	-2819.40	-853.00	143	VCC	3276.60	-853.00	223	COM23	7168.80	840.00	303	SA17	3872.80	840.00
64	GDR	-2743.20	-853.00	144	VCC	3352.80	-853.00	224	COM22	7127.60	840.00	304	SB17	3831.60	840.00
65	VDDB	-2667.00	-853.00	145	VCC	3429.00	-853.00	225	COM21	7086.40	840.00	305	SC17	3790.40	840.00
66	VDDB	-2590.80	-853.00	146	VCC	3505.20	-853.00	226	COM20	7045.20	840.00	306	SA18	3749.20	840.00
67	VDDB	-2514.60	-853.00	147	VCC	3581.40	-853.00	227	COM19	7004.00	840.00	307	SB18	3708.00	840.00
68	VDDB	-2438.40	-853.00	148	VCC	3657.60	-853.00	228	COM18	6962.80	840.00	308	SC18	3666.80	840.00
69	VDD	-2362.20	-853.00	149	VCC	3733.80	-853.00	229	COM17	6921.60	840.00	309	SA19	3625.60	840.00
70	VDD	-2286.00	-853.00	150	VCC	3810.00	-853.00	230	COM16	6880.40	840.00	310	SB19	3584.40	840.00
71	VDD	-2209.80	-853.00	151	VDD	3886.20	-853.00	231	COM15	6839.20	840.00	311	SC19	3543.20	840.00
72	VDD	-2133.60	-853.00	152	VDD	3962.40	-853.00	232	COM14	6798.00	840.00	312	SA20	3502.00	840.00
73	FB	-2057.40	-853.00	153	VDD	4038.60	-853.00	233	COM13	6756.80	840.00	313	SB20	3460.80	840.00
74	VSS	-1981.20	-853.00	154	VDD	4114.80	-853.00	234	COM12	6715.60	840.00	314	SC20	3419.60	840.00
75	RESE	-1905.00	-853.00	155	VDD	4191.00	-853.00	235	COM11	6674.40	840.00	315	SA21	3378.40	840.00
76	VBREF	-1828.80	-853.00	156	VDD	4267.20	-853.00	236	COM10	6633.20	840.00	316	SB21	3337.20	840.00
77	VSS	-1752.60	-853.00	157	VDD	4343.40	-853.00	237	COM9	6592.00	840.00	317	SC21	3296.00	840.00
78	BGGND	-1676.40	-853.00	158	VDD	4419.60	-853.00	238	COM8	6550.80	840.00	318	SA22	3254.80	840.00
79	NC	-1600.20	-853.00	159	VDD	4495.80	-853.00	239	COM7	6509.60	840.00	319	SB22	3213.60	840.00
80	VPA	-1524.00	-853.00	160	VSL	4572.00	-853.00	240	COM6	6468.40	840.00	320	SC22	3172.40	840.00

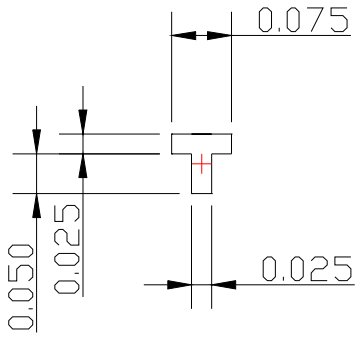
Pad #	Pad Name	X-Axis	Y-Axis
321	SA23	3131.20	840.00
322	SB23	3090.00	840.00
323	SC23	3048.80	840.00
324	SA24	3007.60	840.00
325	SB24	2966.40	840.00
326	SC24	2925.20	840.00
327	SA25	2884.00	840.00
328	SB25	2842.80	840.00
329	SC25	2801.60	840.00
330	SA26	2760.40	840.00
331	SB26	2719.20	840.00
332	SC26	2678.00	840.00
333	SA27	2636.80	840.00
334	SB27	2595.60	840.00
335	SC27	2554.40	840.00
336	SA28	2513.20	840.00
337	SB28	2472.00	840.00
338	SC28	2430.80	840.00
339	SA29	2389.60	840.00
340	SB29	2348.40	840.00
341	SC29	2307.20	840.00
342	SA30	2266.00	840.00
343	SB30	2224.80	840.00
344	SC30	2183.60	840.00
345	SA31	2142.40	840.00
346	SB31	2101.20	840.00
347	SC31	2060.00	840.00
348	SA32	2018.80	840.00
349	SB32	1977.60	840.00
350	SC32	1936.40	840.00
351	SA33	1895.20	840.00
352	SB33	1854.00	840.00
353	SC33	1812.80	840.00
354	SA34	1771.60	840.00
355	SB34	1730.40	840.00
356	SC34	1689.20	840.00
357	SA35	1648.00	840.00
358	SB35	1606.80	840.00
359	SC35	1565.60	840.00
360	SA36	1524.40	840.00
361	SB36	1483.20	840.00
362	SC36	1442.00	840.00
363	SA37	1400.80	840.00
364	SB37	1359.60	840.00
365	SC37	1318.40	840.00
366	SA38	1277.20	840.00
367	SB38	1236.00	840.00
368	SC38	1194.80	840.00
369	SA39	1153.60	840.00
370	SB39	1112.40	840.00
371	SC39	1071.20	840.00
372	SA40	1030.00	840.00
373	SB40	988.80	840.00
374	SC40	947.60	840.00
375	SA41	906.40	840.00
376	SB41	865.20	840.00
377	SC41	824.00	840.00
378	SA42	782.80	840.00
379	SB42	741.60	840.00
380	SC42	700.40	840.00
381	SA43	659.20	840.00
382	SB43	618.00	840.00
383	SC43	576.80	840.00
384	SA44	535.60	840.00
385	SB44	494.40	840.00
386	SC44	453.20	840.00
387	SA45	412.00	840.00
388	SB45	370.80	840.00
389	SC45	329.60	840.00
390	SA46	288.40	840.00
391	SB46	247.20	840.00
392	SC46	206.00	840.00
393	SA47	164.80	840.00
394	SB47	123.60	840.00
395	SC47	82.40	840.00
396	SA48	41.20	840.00
397	SB48	0.00	840.00
398	SC48	-41.20	840.00
399	SA49	-82.40	840.00
400	SB49	-123.60	840.00

Pad #	Pad Name	X-Axis	Y-Axis
401	SC49	-164.80	840.00
402	SA50	-206.00	840.00
403	SB50	-247.20	840.00
404	SC50	-288.40	840.00
405	SA51	-329.60	840.00
406	SB51	-370.80	840.00
407	SC51	-412.00	840.00
408	SA52	-453.20	840.00
409	SB52	-494.40	840.00
410	SC52	-535.60	840.00
411	SA53	-576.80	840.00
412	SB53	-618.00	840.00
413	SC53	-659.20	840.00
414	SA54	-700.40	840.00
415	SB54	-741.60	840.00
416	SC54	-782.80	840.00
417	SA55	-824.00	840.00
418	SB55	-865.20	840.00
419	SC55	-906.40	840.00
420	SA56	-947.60	840.00
421	SB56	-988.80	840.00
422	SC56	-1030.00	840.00
423	SA57	-1071.20	840.00
424	SB57	-1112.40	840.00
425	SC57	-1153.60	840.00
426	SA58	-1194.80	840.00
427	SB58	-1236.00	840.00
428	SC58	-1277.20	840.00
429	SA59	-1318.40	840.00
430	SB59	-1359.60	840.00
431	SC59	-1400.80	840.00
432	SA60	-1565.60	840.00
433	SB60	-1606.80	840.00
434	SC60	-1648.00	840.00
435	SA61	-1689.20	840.00
436	SB61	-1730.40	840.00
437	SC61	-1771.60	840.00
438	SA62	-1812.80	840.00
439	SB62	-1854.00	840.00
440	SC62	-1895.20	840.00
441	SA63	-1936.40	840.00
442	SB63	-1977.60	840.00
443	SC63	-2018.80	840.00
444	SA64	-2060.00	840.00
445	SB64	-2101.20	840.00
446	SC64	-2142.40	840.00
447	SA65	-2183.60	840.00
448	SB65	-2224.80	840.00
449	SC65	-2266.00	840.00
450	SA66	-2307.20	840.00
451	SB66	-2348.40	840.00
452	SC66	-2389.60	840.00
453	SA67	-2430.80	840.00
454	SB67	-2472.00	840.00
455	SC67	-2513.20	840.00
456	SA68	-2554.40	840.00
457	SB68	-2595.60	840.00
458	SC68	-2636.80	840.00
459	SA69	-2678.00	840.00
460	SB69	-2719.20	840.00
461	SC69	-2760.40	840.00
462	SA70	-2801.60	840.00
463	SB70	-2842.80	840.00
464	SC70	-2884.00	840.00
465	SA71	-2925.20	840.00
466	SB71	-2966.40	840.00
467	SC71	-3007.60	840.00
468	SA72	-3048.80	840.00
469	SB72	-3090.00	840.00
470	SC72	-3131.20	840.00
471	SA73	-3172.40	840.00
472	SB73	-3213.60	840.00
473	SC73	-3254.80	840.00
474	SA74	-3296.00	840.00
475	SB74	-3337.20	840.00
476	SC74	-3378.40	840.00
477	SA75	-3419.60	840.00
478	SB75	-3460.80	840.00
479	SC75	-3502.00	840.00
480	SA76	-3543.20	840.00

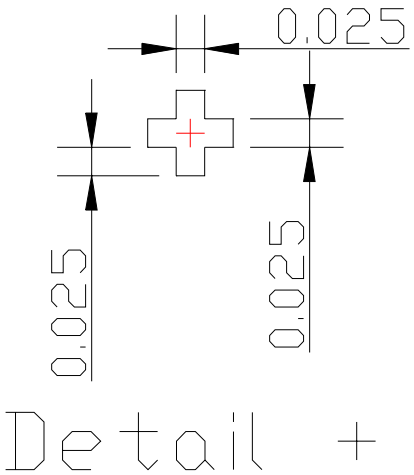
Pad #	Pad Name	X-Axis	Y-Axis
481	SB76	-3584.40	840.00
482	SC76	-3625.60	840.00
483	SA77	-3666.80	840.00
484	SB77	-3708.00	840.00
485	SC77	-3749.20	840.00
486	SA78	-3790.40	840.00
487	SB78	-3831.60	840.00
488	SC78	-3872.80	840.00
489	SA79	-3914.00	840.00
490	SB79	-3955.20	840.00
491	SC79	-3996.40	840.00
492	SA80	-4037.60	840.00
493	SB80	-4078.80	840.00
494	SC80	-4120.00	840.00
495	SA81	-4161.20	840.00
496	SB81	-4202.40	840.00
497	SC81	-4243.60	840.00
498	SA82	-4284.80	840.00
499	SB82	-4326.00	840.00
500	SC82	-4367.20	840.00
501	SA83	-4408.40	840.00
502	SB83	-4449.60	840.00
503	SC83	-4490.80	840.00
504	SA84	-4532.00	840.00
505	SB84	-4573.20	840.00
506	SC84	-4614.40	840.00
507	SA85	-4655.60	840.00
508	SB85	-4696.80	840.00
509	SC85	-4738.00	840.00
510	SA86	-4779.20	840.00
511	SB86	-4820.40	840.00
512	SC86	-4861.60	840.00
513	SA87	-4902.80	840.00
514	SB87	-4944.00	840.00
515	SC87	-4985.20	840.00
516	SA88	-5026.40	840.00
517	SB88	-5067.60	840.00
518	SC88	-5108.80	840.00
519	SA89	-5150.00	840.00
520	SB89	-5191.20	840.00
521	SC89	-5232.40	840.00
522	SA90	-5273.60	840.00
523	SB90	-5314.80	840.00
524	SC90	-5356.00	840.00
525	SA91	-5397.20	840.00
526	SB91	-5438.40	840.00
527	SC91	-5479.60	840.00
528	SA92	-5520.80	840.00
529	SB92	-5562.00	840.00
530	SC92	-5603.20	840.00
531	SA93	-5644.40	840.00
532	SB93	-5685.60	840.00
533	SC93	-5726.80	840.00
534	SA94	-5768.00	840.00
535	SB94	-5809.20	840.00
536	SC94	-5850.40	840.00
537	SA95	-5891.60	840.00
538	SB95	-5932.80	840.00
539	SC95	-5974.00	840.00
540	NC	-6015.20	840.00
541	NC	-6056.40	840.00
542	NC	-6097.60	840.00
543	NC	-6138.80	840.00
544	NC	-6180.00	840.00
545	COM32	-6221.20	840.00
546	COM33	-6262.40	840.00
547	COM34	-6303.60	840.00
548	COM35	-6344.80	840.00
549	COM36	-6386.00	840.00
550	COM37	-6427.20	840.00
551	COM38	-6468.40	840.00
552	COM39	-6509.60	840.00
553	COM40	-6550.80	840.00
554	COM41	-6592.00	840.00
555	COM42	-6633.20	840.00
556	COM43	-6674.40	840.00
557	COM44	-6715.60	840.00
558	COM45	-6756.80	840.00
559	COM46	-6798.00	840.00
560	COM47	-6839.20	840.00

Pad #	Pad Name	X-Axis	Y-Axis
561	COM48	-6880.40	840.00
562	COM49	-6921.60	840.00
563	COM50	-6962.80	840.00
564	COM51	-7004.00	840.00
565	COM52	-7045.20	840.00
566	COM53	-7086.40	840.00
567	COM54	-7127.60	840.00
568	COM55	-7168.80	840.00
569	COM56	-7210.00	840.00
570	COM57	-7251.20	840.00
571	COM58	-7292.40	840.00
572	COM59	-7333.60	840.00
573	COM60	-7374.80	840.00
574	COM61	-7416.00	840.00
575	COM62	-7457.20	840.00
576	COM63	-7498.40	840.00
577	NC	-7560.20	840.00
578	NC	-7568.30	623.18
579	NC	-7568.30	531.18
580	NC	-7568.30	439.18
581	NC	-7568.30	255.18
582	NC	-7568.30	163.18
583	NC	-7568.30	71.18
584	NC	-7568.30	-20.83
585	NC	-7568.30	-112.83
586	NC	-7568.30	-204.83
587	NC	-7568.30	-296.83
588	NC	-7568.30	-388.83
589	NC	-7568.30	-480.83
590	NC	-7568.30	-572.83
591	NC	-7568.30	-664.83

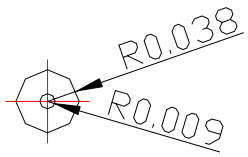
Figure 5-2 : SSD0332Z Alignment mark dimensions



T shape



+ shape



Circle

Unit in um

6 PIN DESCRIPTIONS

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin
Hi-Z = High impedance

Table 6-1 : Pin Descriptions

Pin Name	Pin Type	Description
RES#	I	This pin is reset signal input. When the pin is low, initialization of the chip is executed.
CS#	I	This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
D/C# (SA0)	I	This pin is Data/Command control pin. When the pin is pulled high, the data at D_7-D_0 is treated as data. When the pin is pulled low, the data at D_7-D_0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams in Section 12. In I^2C mode, this pin act as SA0 for slave address selection.
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When I^2C Interface mode is selected, this pin is tied to LOW.
R/W# (WR#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled high and write mode will be carried out when low. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When I^2C Interface mode is selected, this pin is tied to LOW.
D_7-D_0	IO	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D_1 will be the serial data input, SD_{IN}, and D_0 will be the serial clock input, SCLK. When I^2C mode is selected, D_2, D_1 should be tied together and serve as SDA_{out}, SDA_{in} and D_0 is the serial clock input, SCL.
V_{DD}	P	Power Supply pin for logic operation of the driver. It must be connected to external source
V_{SS}	P	Ground pin. It must be connected to external ground.
CL	I	This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. When internal oscillator is disabled, this pin receives display clock signal from external clock source.
CLS	I	This pin is internal clock enable. When this pin is pulled high, internal oscillator is selected. The internal clock will be disabled when it is pulled low, an external clock source must be connected to CL pin for normal operation.
V_{CC}	P	This is the most positive voltage supply pin of the chip. It is supplied either by external high voltage source or internal booster.
V_{COMH}	IO	This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When V_{COMH} is generated internally, a capacitor should be connected between this pin and V_{SS}.
V_{REF}	P	This pin is the reference for OLED driving voltages like $V_{PA,}$ $V_{PB,}$ V_{PC} and V_{COMH}. The relation between V_{REF} and those driving voltages can be programmed and please refer to Table 8-1 : Command Table for details. V_{REF} can be either supplied externally or connected to V_{CC}.
V_{PA}, V_{PB}, V_{PC}	P	These pins are the pre-charge driving voltages for OLED driving segment pins SA0-SA95, SB0-SB95 and SC0-SC95 respectively. They can be supplied externally or internally generated by VP circuit. When internal VP is used, $V_{PA,}$ $V_{PB,}$ V_{PC} pins should be left open.

Pin Name	Pin Type	Description
I_{REF}	IO	This pin is the segment output current reference pin. I_{SEG} is derived from I_{REF} I_{SEG} = Contrast / 256 * I_{REF} * scale factor, in which the contrast is set by command and the scale factor = 1 ~ 16. A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA. Please refer to section 7.4 "Current and Voltage Supply" for the formula of resistor value from I_{REF}.
COM0 ~ COM63	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off.
SA0-SA95, SB0-SB95, SC0-SC95	O	These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off. The 288 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.
FB		This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (Vcc). Please refer to the section 7.12 "DC-DC Voltage Converter" for connection details.
VDDB	P	This is the power supply pin for the internal buffer of the DC-DC voltage converter. 3.5V >= V_{DDB} >= V_{DD}.
VSSB	P	This is the GND pin for the internal buffer of the DC-DC voltage converter. It must be connected to V_{SS}.
GDR	P	This output pin drives the gate of the external NMOS of the booster circuit. Please refer to the section 7.12 "DC-DC Voltage Converter" for connection details.
RESE	I	This pin connects to the source current pin of the external NMOS of the booster circuit. Please refer to the section 7.12 "DC-DC Voltage Converter" for connection details.
VB_{REF}	I	This pin is the internal voltage reference of booster circuit. A stabilization capacitor, typically 1uF, should be connected between VB_{REF} and Vss.
VSL	O	This is segment voltage reference pin. This pin should be left open.
VCL	O	This is common voltage reference pin. This pin should be connected to V_{SS} externally.
TR0-TR8	-	Testing reserved pins. Keep NC.

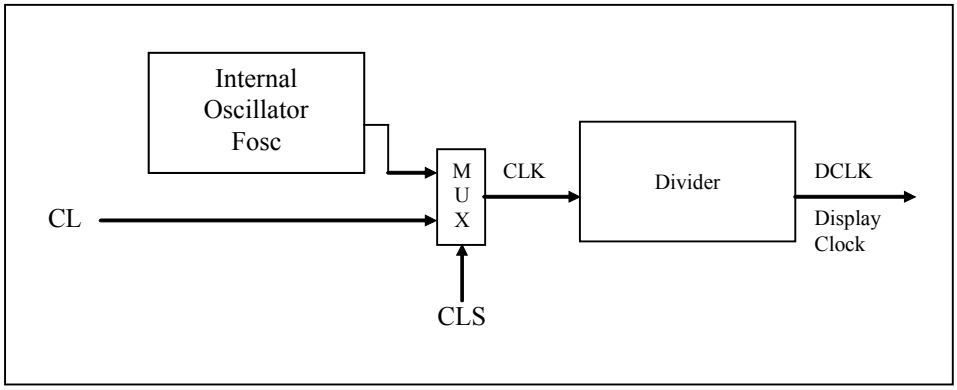
Table 6-2 : MCU Bus Interface Pin Selection

Pin Name	I^2C Interface	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS0	0	0	0	0
BS1	1	0	1	0
BS2	0	1	1	0

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Oscillator Circuit and Display Time Generator

Figure 7-1: Oscillator Circuit



This module is an On-Chip low power RC oscillator circuitry (Figure 7-1). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is high, internal oscillator is selected. If CLS pin is low, external clock from CL pin will be used for CLK. The frequency of internal oscillator Fosc can be programmed by command B3h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor can be programmed from 1 to 16 by command B3h.

7.2 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 64 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Master contrast control register is set at 0FH
9. Individual contrast control registers of color A, B, and C are set at 80H

7.3 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.
If D/C# pin is high, data is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D_0-D_7 is interpreted as a Command and it will be decoded and be written to the corresponding command register.

7.4 Current and Voltage Supply

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} are most positive voltage supply. It can be supplied externally or from internal DC-DC converter.
- V_{DD} are external power supply for logic operation of the driver.
- V_{REF} is reference voltage, which is used to derive driving voltage for segments and commons like $V_{PA,}$ $V_{PB,}$ V_{PC} and V_{COMH}. Normally, V_{REF} is connected to V_{CC}. Please refer to the command table for the relationships of V_{REF} to the segments and commons voltages.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

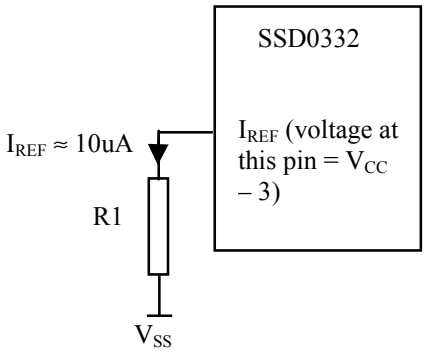
  I_{SEG} = Contrast / 256 * I_{REF} * scale factor

  in which the contrast (0~255) is set by Set Contrast command,
  and the scale factor (1 ~ 16) is set by Master Current Control command.

For example, in order to achieve I_{SEG} = 160uA at maximum contrast 255, I_{REF} is set to around 10uA. This current value is obtained by connecting an appropriate resistor from I_{REF} pin to V_{SS} as shown in Figure 7-2.

Recommended range for Iref = 8 – 12uA

Figure 7-2 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 3V, the value of resistor R1 can be found as below.

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF} = (V_{CC} – 3) / 10uA ≈ 910kΩ for V_{CC} = 12V.

7.5 Segment Drivers/Common Drivers

Segment drivers consists of 288 (96 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted from 0 to 200uA with 256 steps by contrast setting command. Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

Figure 7-3 : Segment and Common Driver Block Diagram

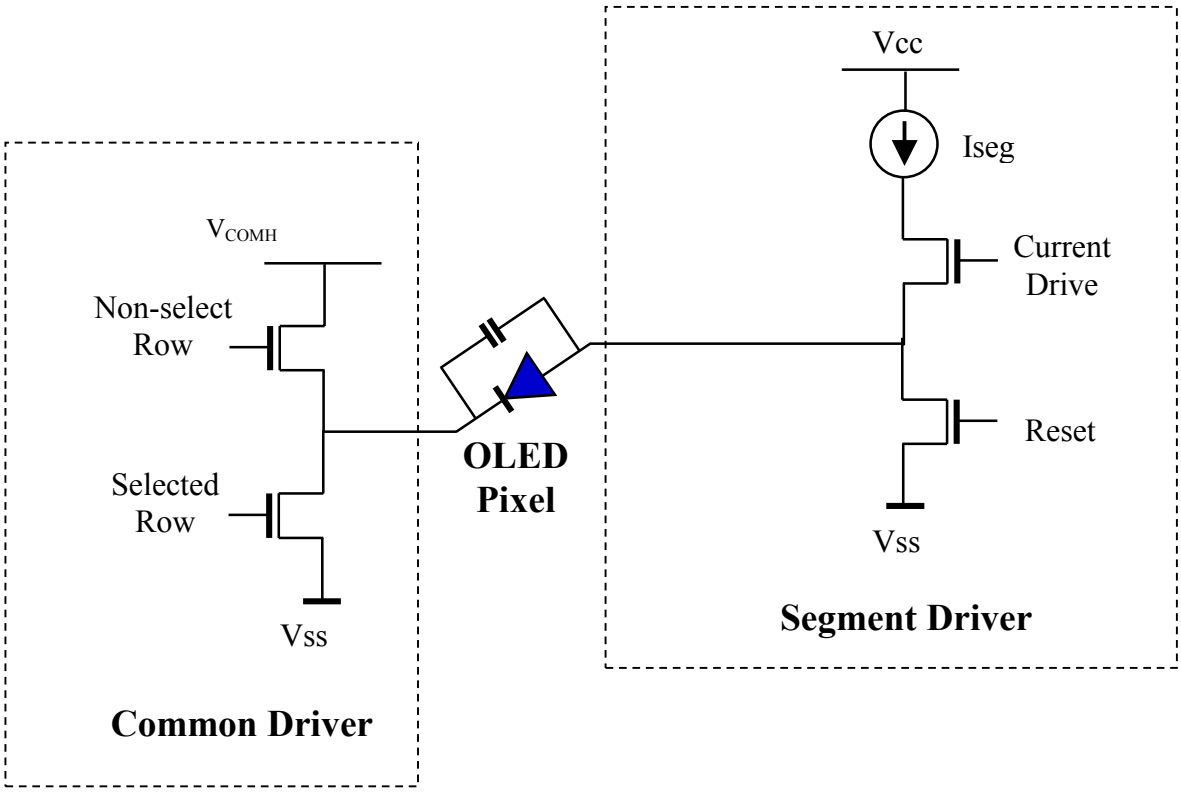
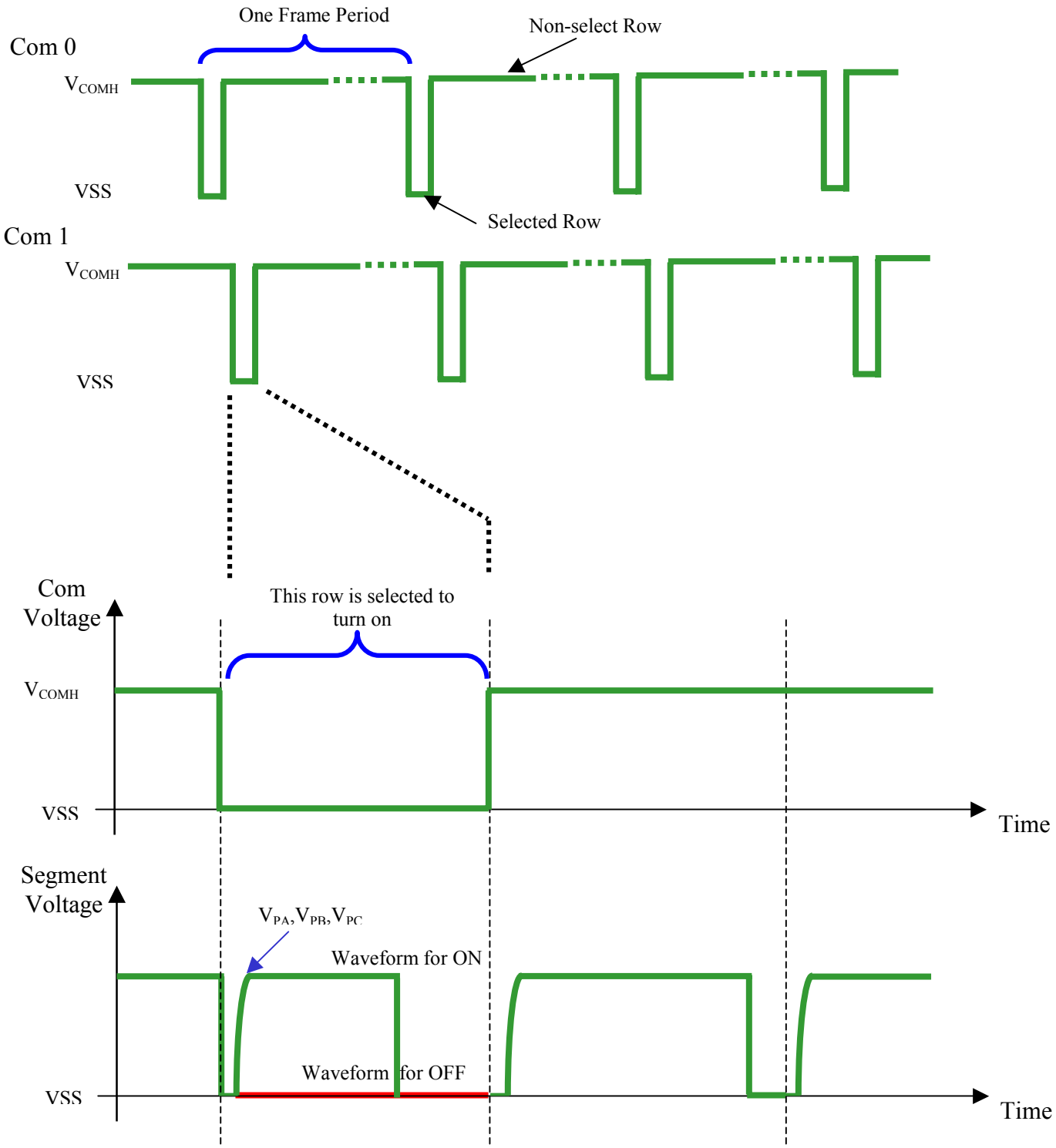


Figure 7-4 : Segment and Common Driver Signal Waveform



The commons are scanned sequentially one by one row. If the row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH}.

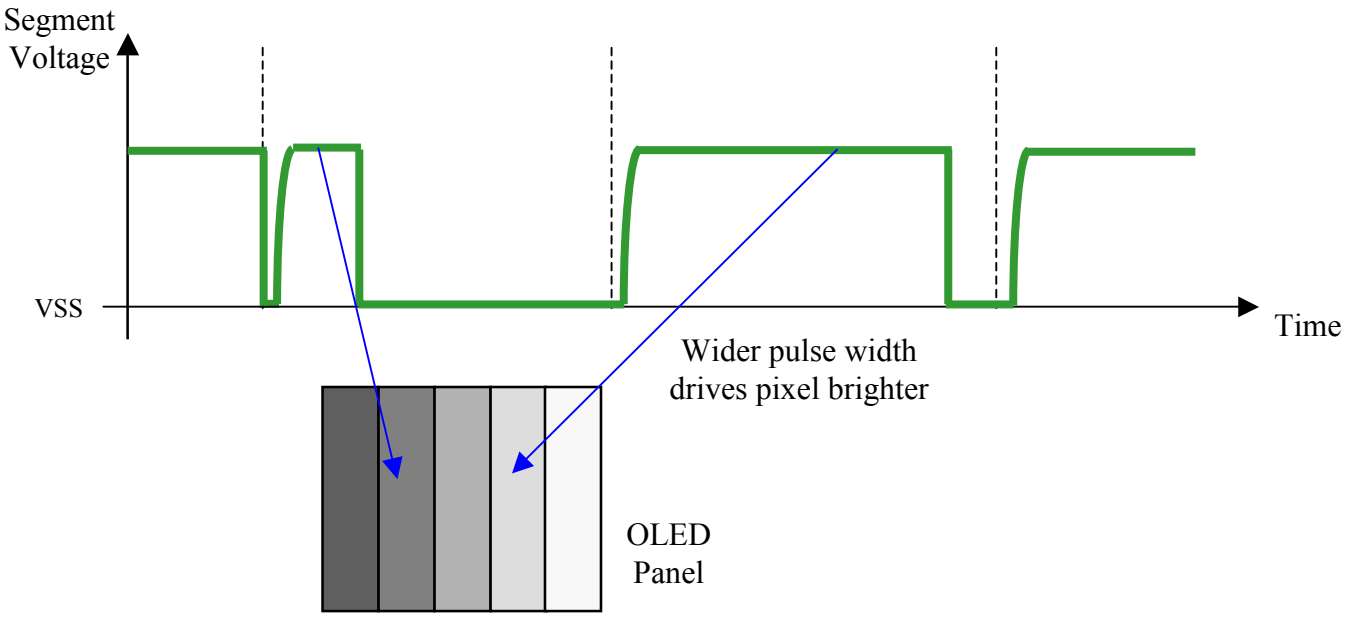
In the scanned row, the pixels on the row will be turned on or off by sending the corresponding data signal to the segment pins. If the pixel is turned off, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned on.

There are three phases to driving a OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{SS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, the pixel is charged up by the segment driver to the desired voltage levels V_{PA}, V_{PB} or V_{PC} for color A, B or C respectively. The period of phase 2 can be programmed by command B1h from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for charging up.

Last phase is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The wider pulse widths in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.

Figure 7-5 : Gray Scale Control by PWM in Segment



The pulse width in current drive stage to control brightness can be programmed through “Set Gray Scale Table” command. It is described in more detailed in section 9 “ Command Descriptions”.

7.6 MPU I^2C Interface

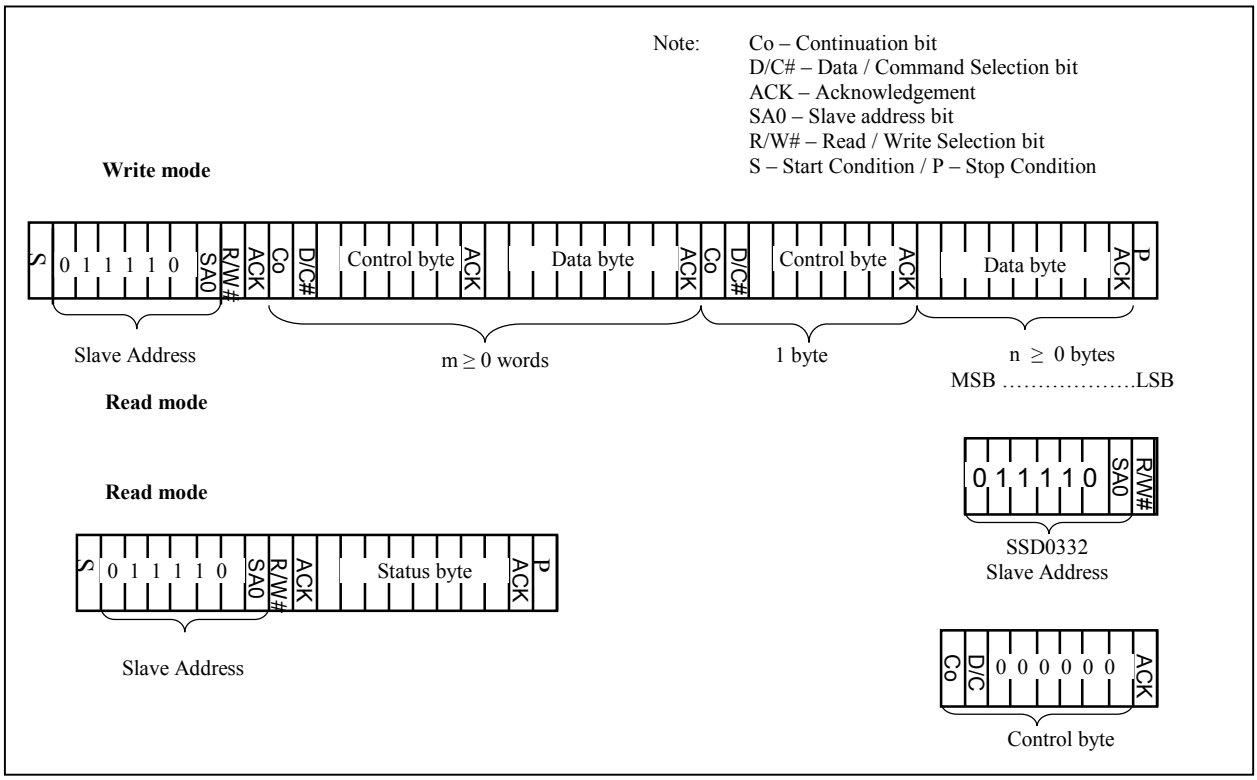
The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (D_2 for output and D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
   SSD0332 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,
   b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
   0 1 1 1 1 0 SA0 R/W#
   "SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD0332.
   "R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.
b) I^2C-bus data signal (SDA)
   SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA. If SDA in is connected to the "SDA out", the device becomes fully I^2C bus compatible.
   It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
   The "SDA out" pin may be disconnected from the "SDA in" pin. With such arrangement, the acknowledgement signal will be ignored in the I^2C-bus.
c) I^2C-bus clock signal (SCL)
   The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

7.6.1 I²C-bus Write data and read register status

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 7-6 for the write mode of I²C-bus in chronological order.

Figure 7-6 : I²C-bus data format



7.6.2 Write mode for I^2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 7-7. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD0332, the slave address is either "b0111100" or "b0111101" by changing the SA0 to HIGH or LOW.
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7-8 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 7-7. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 7-7 : Definition of the Start and Stop Condition

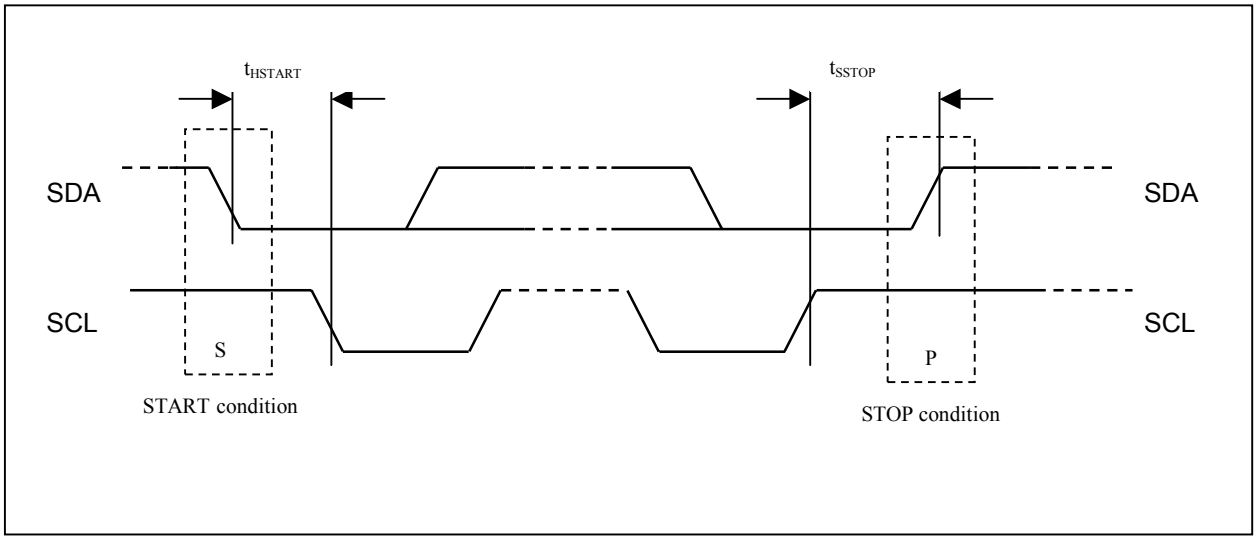
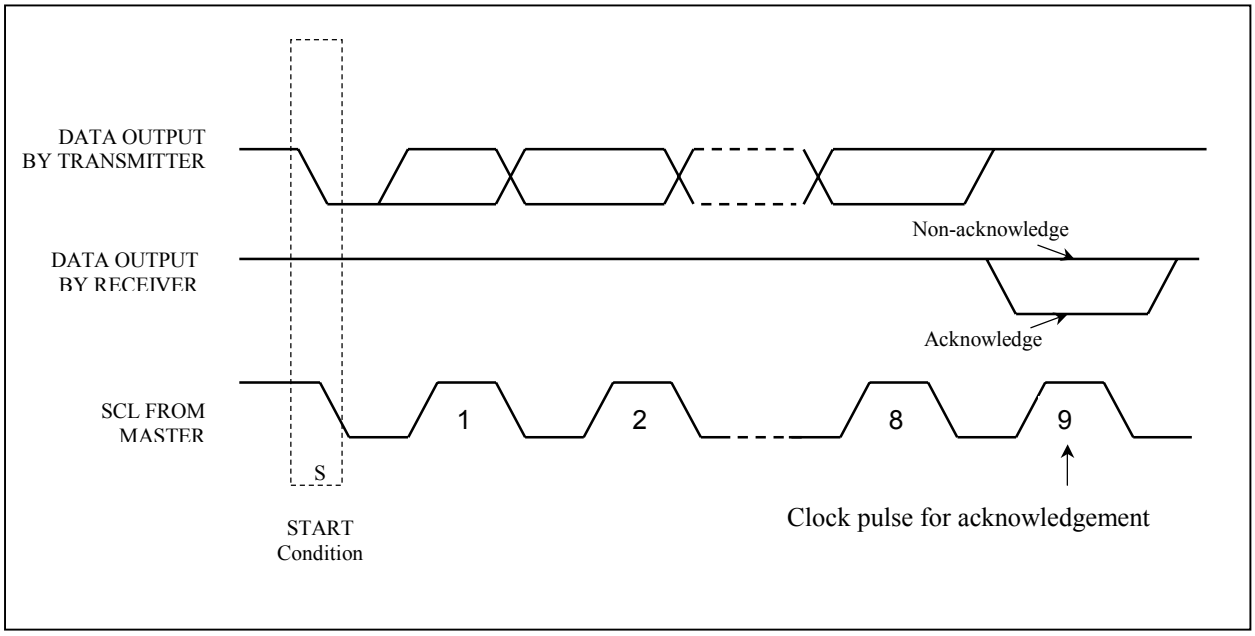


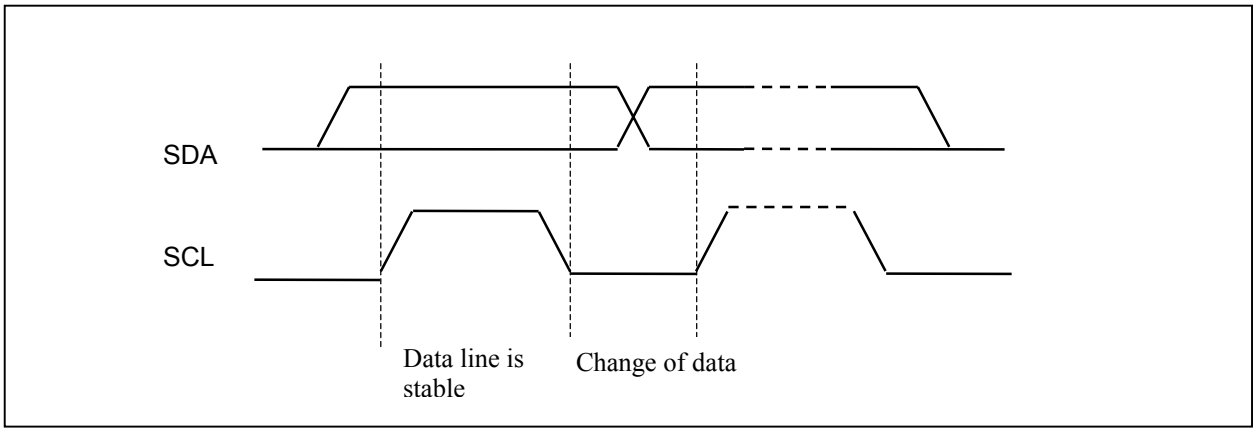
Figure 7-8 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 7-9 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 7-9 : Definition of the data transfer condition



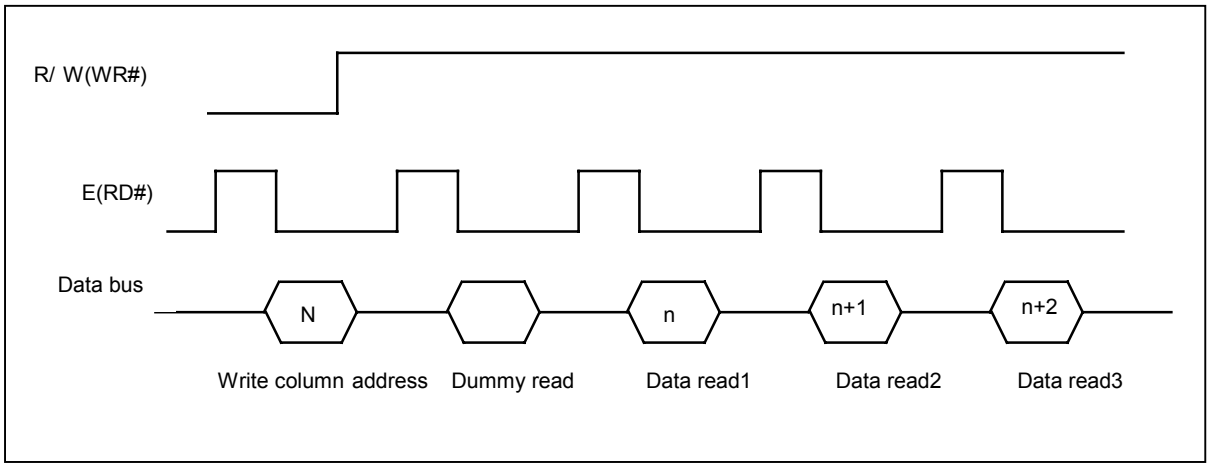
7.6.3 Read mode for I^2C (Read status register)

1) The master device firstly initiates the data communication by a start condition. The definition of the start condition is shown in Figure 7-7.
2) The slave address is following the start condition for recognition use. For the SSD0332, the slave address is either "b0111100" or "b0111101".
3) The read mode is established by setting R/W# bit to logic "1". The read mode allows the MCU to monitor the internal status of the chip.
4) An acknowledgement signal will be generated after sending one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 7-8 for the graphical representation of the acknowledge signal.
5) The status of the register will be read at the next status byte. Please refer to the Table 8-2 : Read Command Table for the explanation of the status byte.
6) The read mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 7-7.

7.7 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), R/W(WR#), D/C, E (RD#) and CS#. R/W(WR#) High Input indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W(WR#) Low Input indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The E(RD#) input serves as data latch signal (clock) when high provided that CS# is low. Refer to Figure 12-2 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.
In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-10 below.

Figure 7-10 : Display data read back procedure - insertion of dummy read



7.8 MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), E (RD#), R/W(WR#), D/C and CS#. The E(RD#) input serves as data read latch signal (clock) when low, provided that CS# is low. Display data RAM or status register read is controlled by D/C#.

R/W(WR#) input serves as data write latch signal (clock) when low provided that CS# is low, or CS# input serves as data write latch signal at rising edge when R/W(WR#) is low. Display data RAM or command register write is controlled by D/C. Refer to Figure 12-3 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

7.9 MPU Serial Interface

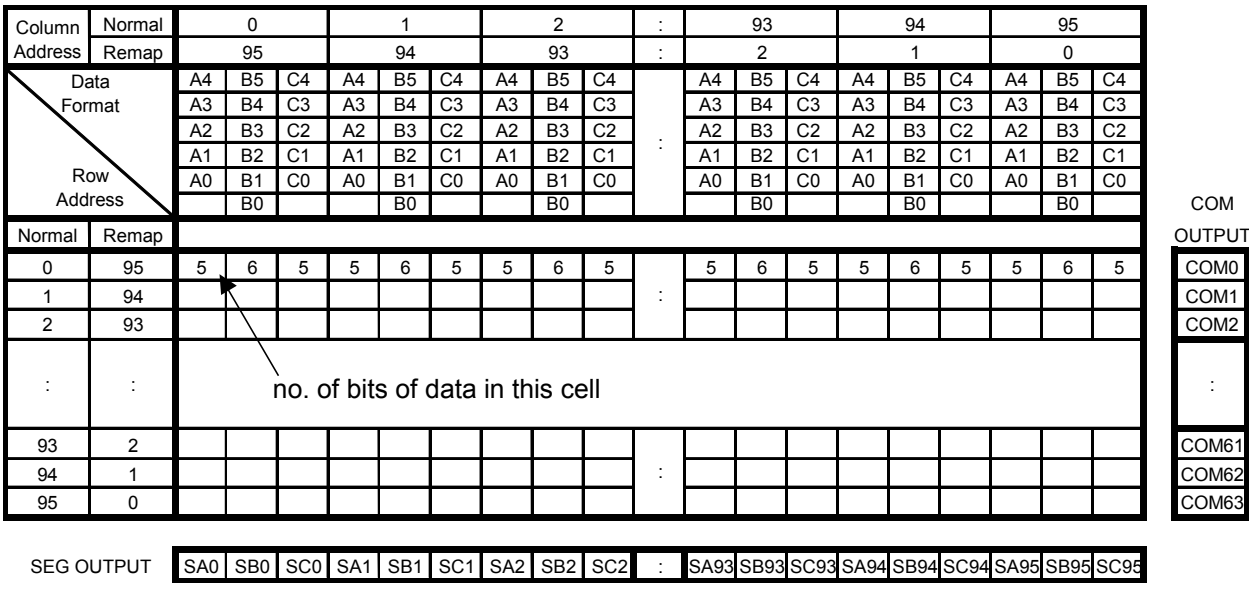
The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. D3 to D7, E and R/W pins can be connected to external ground.

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D_7, D_6, ... D_0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

7.10 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The size of the RAM is 96 x 64 x 16bits.
For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.
For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.
Each pixel has 16-bit data. Three sub-pixels for color A, B and C have 6 bits, 5 bits and 6 bits respectively. The arrangement of data pixel in graphic display data RAM is shown below.

Figure 7-11 : 65k Color Depth Graphic Display Data RAM Structure



The sequence of sending one pixel of 16-bit data is divided into two 8-bit sessions as shown below.

Figure 7-12 : 65k Color Depth Graphic Display Data Writing Sequence

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1st byte	C4	C3	C2	C1	C0	B5	B4	B3
2nd byte	B2	B1	B0	A4	A3	A2	A1	A0

In 256-color mode, each pixel is composed of 8-bit. Color A uses 2-bit while color B and color C each is represented by 3-bit. Although only 8 bits are required to represent one pixel, each pixel occupies 16-bit space inside graphic display data RAM with format as follows.

For 256-color mode, one pixel data is sent in a 8-bit session like below.

Figure 7-13 : 256 Color Depth Graphic Display Data Writing Sequence

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1st byte	C2	C1	C0	B2	B1	B0	A1	A0

Figure 7-14 : 256 Color Depth Graphic Display Data RAM Structure for One Pixel

Color C (3 bits)	RAM Content (5 bits)
000	00000
001	00100
010	01000
011	01100
100	10010
101	10110
110	11010
111	11110

Color B (3 bits)	RAM Content (6 bits)
000	000000
001	001000
010	010000
011	011000
100	100100
101	101100
110	110100
111	111100

Color A (2 bits)	RAM Content (5 bits)
00	00000
01	01000
10	10100
11	11100

7.11 Gray Scale and Gray Scale Table

The gray scale display is produced by controlling the current pulse widths from the segment driver in the current drive phase. The gray scale table stores the corresponding pulse widths (PW0 ~ PW63) of the 64 gray scale levels (GS0~GS63). The wider the pulse width, the brighter the pixel will be. This single gray scale table supports all the three colors A, B and C. The pulse widths are entered by software commands.

As shown in Figure 7-15, color B sub-pixel RAM data has 6 bits, represent the 64 gray scale levels from GS0 to GS63. color A and color C sub-pixel RAM data has only 5 bits, represent 32 gray scale levels from GS0, GS2, …, GS62.

Figure 7-15 : Relation between graphic data RAM value and gray scale table entry for three colors in 65K color mode

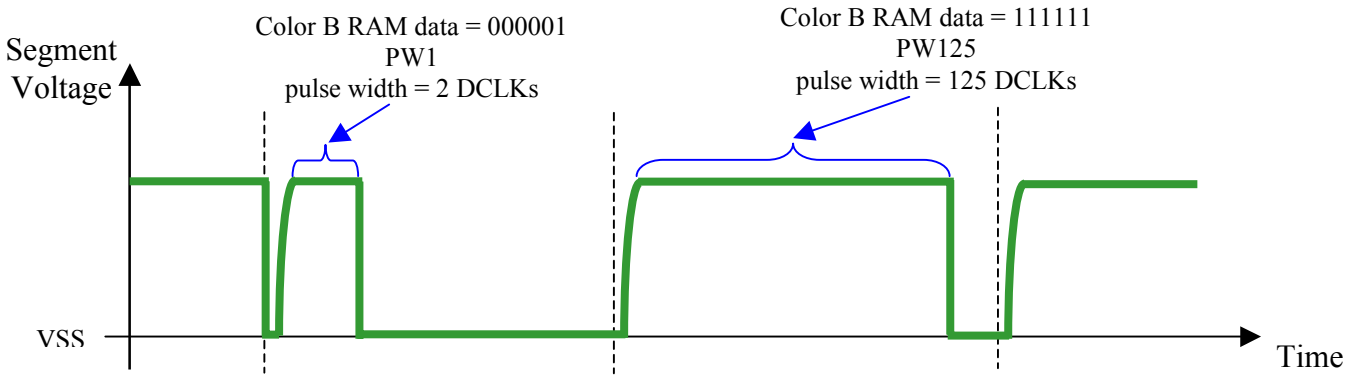
Color A, C , RAM data (5 bits)	Color B, RAM data (6 bits)	Gray Scale
0	0	GS0
-	1	GS 1
1	2	GS 2
-	3	GS 3
2	4	GS 4
:	:	:
:	:	:
30	60	GS 60
-	61	GS 61
31	62	GS 62
-	63	GS 63

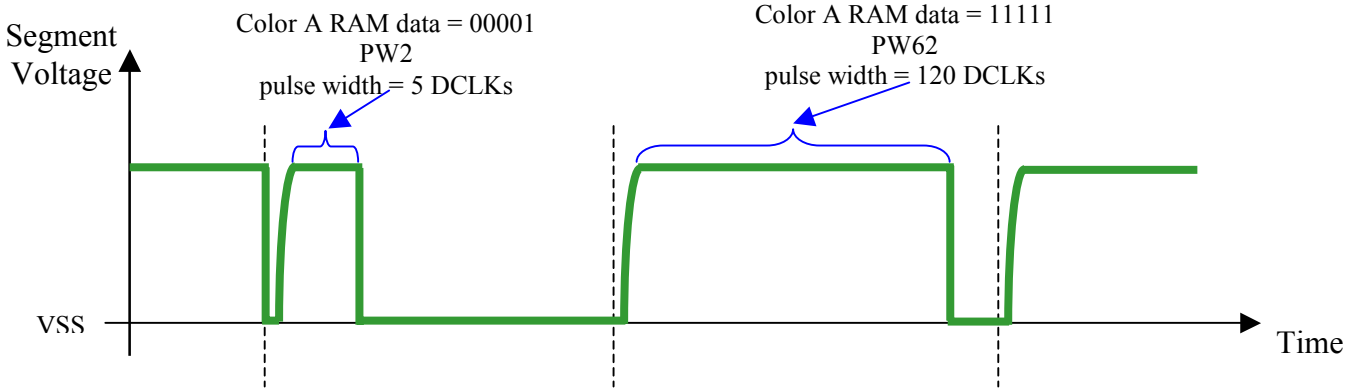
The meaning of values inside data RAM with respect to the gray scale level is best to be illustrated in an example below.

Gray Scale (Pulse Width)	Value/DCLKs
PW0	0
PW1	2
PW2	5
:	:
PW62	120
PW63	125

Gray Scale Table

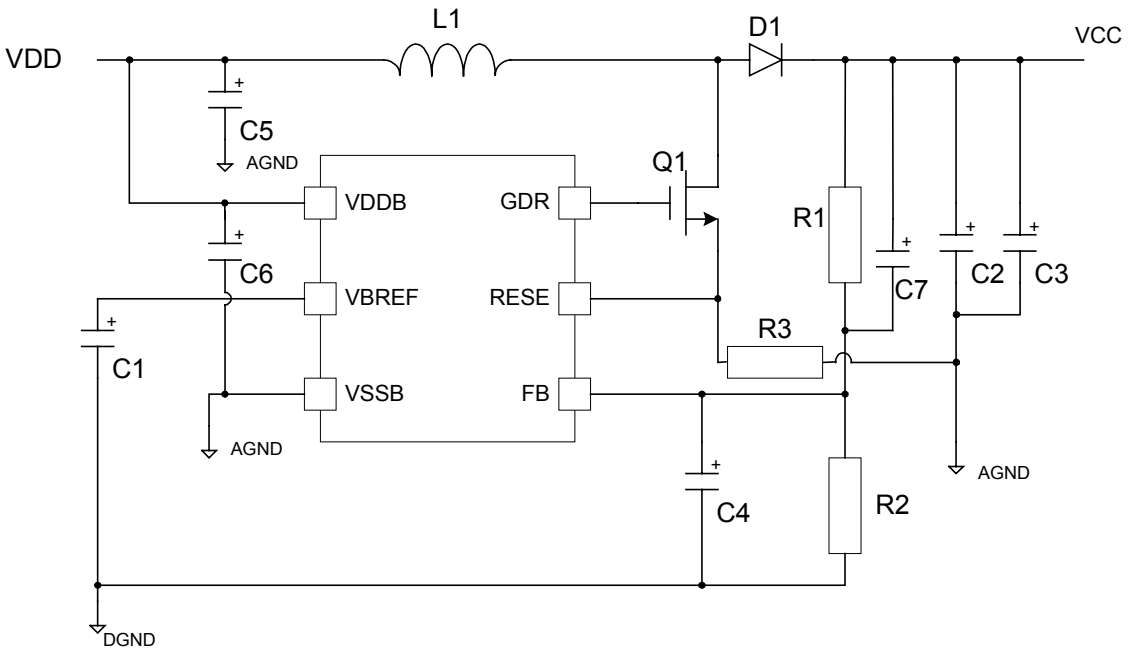
Figure 7-16 : Illustration of relation between graphic display RAM value and gray scale control





7.12 DC-DC Voltage Converter

Figure 7-17 : DC-DC Converter Application Circuit Diagram



It is a switching voltage generator circuit, designed for handheld applications. In SSD0332, internal DC-DC voltage converter accompanying with an external application circuit (shown in Figure 7-17) can generate a high voltage supply V_{CC} from a low voltage supply input V_{DD}. V_{CC} is the voltage supply to the OLED driver block. The application circuit above is an example for the input voltage of 3V V_{DD} to generate V_{CC} of 12V @20mA ~ 30mA application.

*All paths to AGND should be connected as short as possible

Passive components selection:

Table 7-1 : Components Selection for DC-DC Converter

Components	Typical Value	Remark
L1	Inductor, 22uH	2A
D1	Schottky diode	2A, 25V e.g. 1N5822
Q1	MOSFET	N-FET with low R_{DS}(on) and low Vth voltage. e.g. MGSF1N02LT1 [ON SEMICONDUCTOR]
R1, R2	Resistor	1%,1/10W
R3	Resistor, 1.2Ω	1%, 1/2W
C1	Capacitor, 1uF	16V
C2	Capacitor, 22uF	Low ESR, 25V
C3	Capacitor, 1uF	16V
C4	Capacitor, 10nF	16V
C5	Capacitor, 1 ~ 10 uF	16V
C6	Capacitor, 0.1 ~ 1uF	16V
C7	Capacitor, 15nF	16V

The VCC output voltage level can be adjusted by R1 and R2, the reference formula is:

VCC = 1.2 x (R1+R2) / R2

8 COMMAND TABLE

Table 8-1 : Command Table

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#) = 0, E (RD#)=1**)**

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0	15 A[6:0] B[6: 0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	A[6:0] sets the column start address from 0-95, POR=00d. B[6:0] sets the column end address from 0-95 POR=95d.
0 0 0	75 A[5:0] B[5:0]	0 * *	1 * *	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	A[5:0] sets the row start address from 0-63, POR=00d. B[5:0] sets the row end address from 0-63, POR=63d.
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast for Color A (Segment Pins :SA0 – SA95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H
0 0	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Contrast for Color B (Segment Pins :SB0 – SB95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H
0 0	83 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Contrast for Color C (Segment Pins :SC0 – SC95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. POR = 80H
0 0	87 A[3:0]	1 *	0 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Current Control	Set A[3:0] from 0000, 0001… to 1111 to adjust the master current attenuation factor from 1/16, 2/16… to 16/16. POR =1111b, for no attenuation.
0 0	A0 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 *	0 *	0 A_1	0 A_0	Set Re-map & Data Format	A[0]=0, Horizontal address increment (POR) A[0]=1, Vertical address increment A[1]=0, Column address 0 is mapped to SEG0 (POR) A[1]=1, Column address 95 is mapped to SEG0 A[4]=0, Scan from COM 0 to COM [N –1] A[4]=1, Scan from COM [N-1] to COM0. Where N is the Multiplex ratio. A[5]=0, Disable COM Split Odd Even (POR) A[5]=1, Enable COM Split Odd Even A[7:6]=00; 256 color format = 01; 65k color format(POR)
0 0	A1 A[5:0]	1 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-63. Display start line register is reset to 00H after POR.

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	A2	1	0	1	0	0	0	1	0	Set Display Offset	Set vertical scroll by COM from 0-63.
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		The value is reset to 00H after POR.
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h=Normal Display (POR) A5h=Entire Display On, all pixels turn on at GS level 63 A6h=Entire Display Off, all pixels turn off A7h=Inverse Display
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	The next command determines multiplex
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		ratio N from 16MUX-64MUX, POR=63d (64MUX) A[5:0]=0-14d (invalid entry)
0	AD	1	0	1	0	1	1	0	1	Set Master Configuration	A[0]=0, Select external VCC supply at Display ON
0	A[7:0]	1	0	0	0	1	A_2	A_1	A_0		A[0]=1, Select internal booster at Display ON (POR) A[1]=0, Select external VCOMH voltage supply at Display O A[1]=1, Select internal VCOMH regulator at Display ON (PO A[2]=0, Select External VP voltage supply A[2]=1, Select Internal VP (POR)
0	AE~AF	1	0	1	0	X_3	1	1	1	Set Display On/Off	AEh=Display off (POR) AFh=Display on
0	B0	1	0	1	1	0	0	0	0	Set Power Save	A[7:0]=00 (POR)
0	A[7:0]	0	0	0	A_4	0	0	A_1	0		A[7:0]=12, power saving mode
0	B1	1	0	1	1	0	0	0	1	Phase 1 and 2 period adjustment	A[3:0] Phase 1 period in 1~16 DCLK clocks [POR=4h]
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:4] Phase 2 period in 1~16 DCLK clocks [POR=7h]
0	B3	1	0	1	1	0	0	1	1	Display Clock Divider / Oscillator Frequency	A[3:0] [DIVIDER, POR=0]
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		DCLK is generated from CLK divided by DIVIDER +1 (i.e., A[7:4] Fosc frequency, POR=D0H Frequency increases as level increases
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next 32 bytes of command set the current drive pulse widt
0	A[7:0]--PW1	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		gray scale level GS1, GS3, GS5 …GS63 as below:
0	B[7:0]--PW3	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		A[7:0]=PW1, POR=1, it equals 1 DCLK clock B[7:0]=PW3, POR=5, it equals 3 DCLK clocks
0	C[7:0]--PW5	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		C[7:0]=PW5, POR= 9
0	:										:
0	:										:
0	:										AE[7:0]=PW61, POR=121 AF[7:0]=PW63, POR=125, it equals 125 DCLK clocks
0	AE[7:0]--PW61	AE_7	AE_6	AE_5	AE_4	AE_3	AE_2	AE_1	AE_0		**Note** (1) GS0 has no pre-charge and current drive stages.
0	AF[7:0]--PW63	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0		For GS2 GS4…GS62, they are derived by driver itself with: $PWn = (PWn_{-1}+PWn_{+1})/2$ Max pulse width is 125

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	B9	1	0	1	1	1	0	0	1	Enable Linear Gray Scale Table	Enable build-in linear gray scale table (POR=Enable) PW1=1,PW2=3,PW3=5 … PW61=121,PW62=123,PW63=125
0 0	BB ~ BD A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	1 A_3	X_2 A_2	X_1 A_1	X_0 A_0	V_{PA}, V_{PB}, V_{PC} level setting for Color A,B,C	011b for Color A, 100b for Color B, 101b for Color C A[7:0] 00000000 0.43*Vref 00111111 0.83*Vref 01111111 1.0*Vref 1xxxxxxx connects to VCOMH (POR)
0 0	BE A[6:0]	1 *	0 A_6	1 A_5	1 A_4	1 A_3	1 A_2	1 A_1	0 A_0	Set V_{COMH}	A[6:0] 0000000 0.43*Vref 0111111 0.83*Vref (POR)
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Graphic Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	21	0	0	1	0	0	0	0	1	Draw Line	A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		E[5:1] : Color C of the line
0	E[5:1]	*	*	E_5	E_4	E_3	E_2	E_1	*		F[5:0] : Color B of the line
0	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		G[5:1] : Color A of the line
0	G[5:1]	*	*	G_5	G_4	G_3	G_2	G_1	*		
0	22	0	0	1	0	0	0	1	0	Drawing Rectangle	A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		E[5:1] : Color C of the line
0	E[5:1]	*	*	E_5	E_4	E_3	E_2	E_1	*		F[5:0] : Color B of the line
0	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		G[5:1] : Color A of the line
0	G[5:1]	*	*	G_5	G_4	G_3	G_2	G_1	*		H[5:1] : Color C of the fill area
0	H[5:1]	*	*	H_5	H_4	H_3	H_2	H_1	*		I[5:0] : Color B of the fill area
0	I[5:0]	*	*	I_5	I_4	I_3	I_2	I_1	I_0		J[5:1] : Color A of the fill area
0	J[5:1]	*	*	J_5	J_4	J_3	J_2	J_1	*		
0	23	0	0	1	0	0	0	1	1	Copy	A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		E[6:0] : Column Address of New Start
0	E[6:0]	*	E_6	E_5	E_4	E_3	E_2	E_1	E_0		F[5:0] : Row Address of New Start
0	F[5:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		
0	24	0	0	1	0	0	1	0	0	Dim Window	A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15
0	25	0	0	1	0	0	1	0	1	Clear Window	A[6:0] : Column Address of Start
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		B[5:0] : Row Address of Start
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		C[6:0] : Column Address of End
0	C[6:0]	*	C_6	C_5	C_4	C_3	C_2	C_1	C_0		D[5:0] : Row Address of End
0	D[5:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		
0	26	0	0	1	0	0	1	1	0	Fill Enable / Disable	A0 0 : Disable Fill for Draw Rectangle Command (POR) 1 : Enable Fill for Draw Rectangle Command A[3:1] 000 : Reserved values A4 0 : Disable reverse copy (POR) 1 : Enable reverse during copy command.
0	A[4:0]	*	*	*	A_4	0	0	0	A_0		

Table 8-2 : Read Command Table

(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read *	D_7 : "1" for Command lock D_6 : "1" for display OFF / "0" for display ON D_5 : Reserve D_4 : Reserve D_3 : Reserve D_2 : Reserve D_1 : Reserve D_0 : Reserve

Note

(1) Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

8.1 Data Read / Write

To read data from the GDDRAM, input HIGH to R/W (WR#) pin and D/C pin for 6800-series parallel mode, LOW to E (RD#) pin and HIGH to D/C pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read. See Figure 7-10 in Functional Block Description.

To write data to the GDDRAM, input LOW to R/W (WR#) pin and HIGH to D/C pin for 6800-series parallel mode AND 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

Table 8-3 : Address increment table (Automatic)

D/C	R/W (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

9 COMMAND DESCRIPTIONS

9.1 Fundamental Command

9.1.1 Set Column Address (15h)

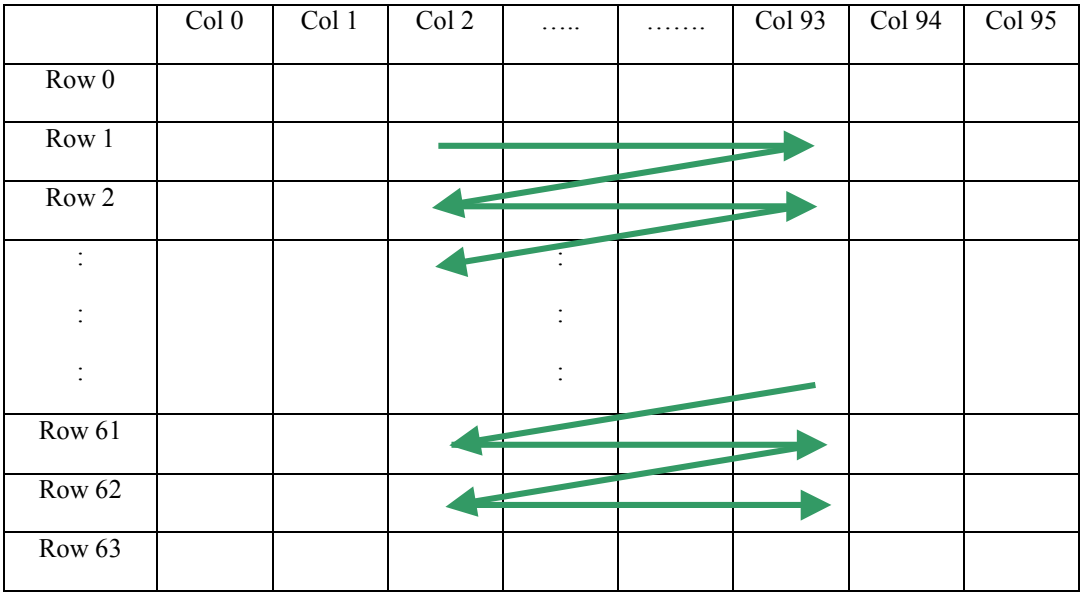
This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address.

9.1.2 Set Row Address (75h)

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

For example, column start address is set to 2 and column end address is set to 93, row start address is set to 1 and row end address is set to 62. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 93 and from row 1 to row 62 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation. Whenever the column address pointer finishes accessing the end column 93, it is reset back to column 2 and row address is automatically increased by 1. While the end row 62 and end column 93 RAM location is accessed, the row address is reset back to 1. The diagram below shows the way of column and row address pointer movement for this example.

Figure 9-1 : Example of Column and Row Address Pointer Movement



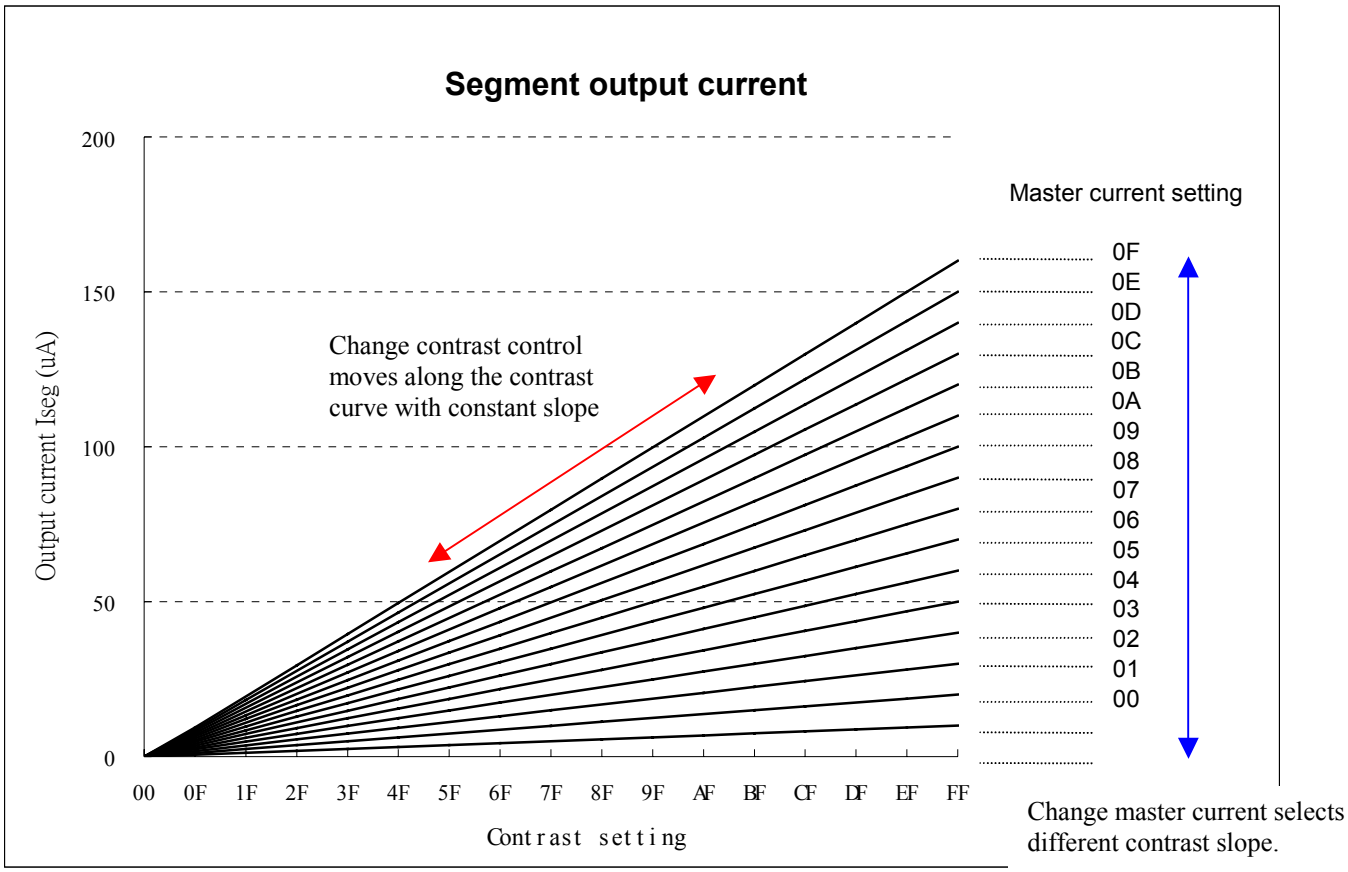
9.1.3 Set Contrast for Color A, B, C (81h, 82h, 83h)

This command is to set Contrast Setting of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter of the color. This relation is shown in Figure 9-2. In many situations, the output brightness of color A, B and C pixels are different under the same segment current condition. The contrasts of color A, B and C are set such that the brightness of each color are the same on the OLED panel

9.1.4 Master Current Control (87h)

This command is to control the segment output current by a scale factor. This factor is common to color A, B and C. The chip has 16 master control steps. The factor is ranged from 1 [0000] to 16 [1111]. POR is 16 [1111]. The smaller the master current value, the dimmer the OLED panel display is set. For example, if original segment output current of a color is 160uA at scale factor = 16, setting scale factor to 8 to reduce the current to 80uA. Please see Figure 9-2.

Figure 9-2 : Segment Output Current for Different Contrast Control and Master Current Setting

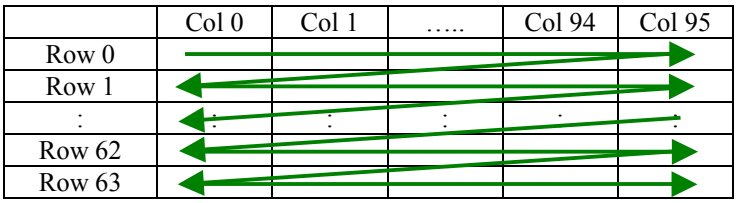


9.1.5 Set Re-map & Data Format (A0h)

This command has multiple configurations and each bit setting is described as follows.

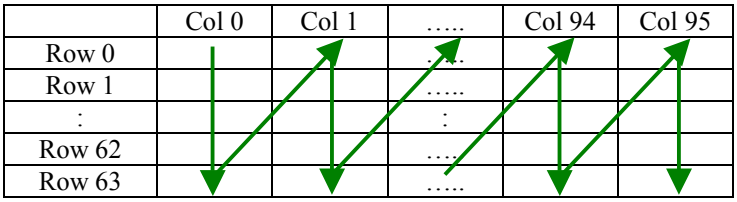
- Address increment mode (A[0])
  When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 9-4.

Figure 9-3 : Address Pointer Movement of Horizontal Address Increment Mode



When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 9-4.

Figure 9-4 : Address Pointer Movement of Vertical Address Increment Mode



- Column Address Mapping (A[1])
  This command bit is made for flexible layout of segment signals in OLED module with segment arranged from left to right or vice versa.

- COM Remap (A[4])
  This bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.

- Odd even split of COM pins (A[5])
  This bit can set the odd even arrangement of COM pins.
  A[5] = 0: Disable COM split odd even, pin assignment of common is in sequential as
  COM63 COM62 .... COM 33 COM32..SC95..SA0..COM0 COM1.... COM30 COM31
  A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
  COM63 COM61.... COM3 COM1..SC95..SA0..COM0 COM2.... COM60 COM62

- Display color mode (A[7:6])
  Select either 65k or 256 color mode. The display RAM data format in different mode is described in section “Graphic Display Data RAM (GDDRAM)”.

9.1.6 Set Display Start Line (A1h)

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 9-5 : Example of Set Display Start Line with no Remap

	64	64	62	62	Mux ratio
COM Pin	0	4	0	4	Display start line
COM0	Row0	Row4	Row0	Row4	
COM1	Row1	Row5	Row1	Row5	
COM2	Row2	Row6	Row2	Row6	
COM3	Row3	Row7	Row3	Row7	
:	:	:	:	:	
:	:	:	:	:	
COM57	Row57	Row61	Row57	Row61	
COM58	Row58	Row62	Row58	Row62	
COM59	Row59	Row63	Row59	Row63	
COM60	Row60	Row0	Row60	Row0	
COM61	Row61	Row1	Row61	Row1	
COM62	Row62	Row2	-	-	
COM63	Row63	Row3	-	-	

9.1.7 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-63. For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second command should be given by 0010000. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 9-6 : Example of Set Display Offset with no Remap

	64	64	62	62	Mux ratio
COM Pin	0	4	0	4	Display offset
COM0	Row0	Row4	Row0	Row4	
COM1	Row1	Row5	Row1	Row5	
COM2	Row2	Row6	Row2	Row6	
COM3	Row3	Row7	Row3	Row7	
:	:	:	:	:	
:	:	:	:	:	
COM57	Row57	Row61	Row57	Row61	
COM58	Row58	Row62	Row58	-	
COM59	Row59	Row63	Row59	-	
COM60	Row60	Row0	Row60	Row0	
COM61	Row61	Row1	Row61	Row1	
COM62	Row62	Row2	-	Row2	
COM63	Row63	Row3	-	Row3	

9.1.8 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display.

- Set Entire Display On (A5h)
  Forces the entire display to be at "GS63" regardless of the contents of the display data RAM.
- Set Entire Display Off (A6h)
  Forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM.
- Inverse Display (A7h)
  The gray level of display data are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", ….
- Normal Display (A4h)
  Reset the above effect and turn the data to ON at the corresponding gray level.

9.1.9 Set Multiplex Ratio (A8h)

This command switches default 1:64 multiplex mode to any multiplex mode from 16 to 64. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h.

9.1.10 Set Master Configuration (ADh)

This command contains multiple bits to control several functionalities of the driver.

- Select DC-DC converter (A[0])
  0 = Disable selection of DC-DC converter and VCC is supplied externally.
  1 (POR) = Enable selection of DC-DC converter to supply high voltage to VCC. The output voltage of the converter is set by values of external resistors. Please refer to section 7.12 "DC-DC Voltage Converter" for details.
- Select V_{COMH} supply (A[1])
  0 = Select external V_{COMH} voltage from V_{COMH} pin for the common waveform high voltage level supply. It is recommended to set the voltage of V_{COMH} such that the OLED pixel diode is not turned on (prefer in reverse bias state) when the segment pin is either driven to V_{PA}, V_{PB} or V_{PC} level.
  1 = Select internal V_{COMH} voltage generated by regulator from V_{REF}. The level of V_{COMH} can be programmed by command BEh.
- Select pre-charge voltage supply (A[2])
  0 = Select pre-charge voltage sources from external pins V_{PA}, V_{PB}, V_{PC} for color A, B and C respectively.
  1 = Select pre-charge voltage supply internally. The level of V_{PA}, V_{PB}, V_{PC} can be set by command BBh, BCh and BDh for color A, B and C respectively.

9.1.11 Set Display On/Off (AEh/AFh)

These single byte commands are used to turn the OLED panel display on or off. When the display is on, the selected circuits by Set Master Configuration command will be turned on. When the display is off, those circuits will be turned off and the segment and common output are in high impedance state.

9.1.12 Phase 1 and 2 Period Adjustment (B1h)

This command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 1 to 16 in the unit of DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 1 to 16 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_{PA}, V_{PB}, V_{PC} for color A, B and C respectively.

9.1.13 Set Display Clock Divide Ratio/ Oscillator Frequency (B3h)

This command consists of two functions:

- Display Clock Divide Ratio (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with power on reset value = 1. Please refer to section "Oscillator Circuit and Display Time Generator" for the details of DCLK and CLK.
- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency setting available as shown below. The default value is 1101b which represents 0.97MHz Fosc.

9.1.14 Set Gray Scale Table (B8h)

This command is used to set the gray scale table for the display. Except gray scale entry 0, which is zero as it has no pre-charge and current drive, each odd entry gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter is the OLED pixel when it's turned on. Please refer to section "Graphic Display Data RAM (GDDRAM)" for more detailed explanation of relation of display data RAM, gray scale table and the pixel brightness.

Following the command B8h, the user has to set the pulse width from PW1, PW3, PW5, …, PW59, PW61, PW63 one by one in sequence and complies the following conditions.

$$PW1 > 0;\ PW3 > PW1 + 1;\ PW5 > PW3 + 1;\ \ldots\ldots$$

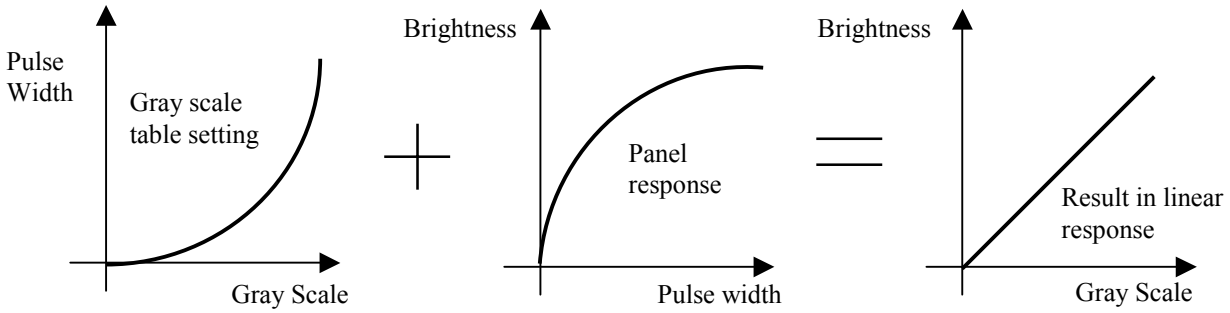
Afterwards, the driver automatically derives the pulse width of even entry of gray scale table PW2, PW4, …, PW62 with the formula like below.

$$PWn = (PWn\text{-}1 + PWn+1) / 2$$

For example, if PW1 = 3 DCLKs and PW3 = 7 DCLKs, PW2 = (3+7)/2 = 5 DCLKs

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

Figure 9-7 : Example of gamma correction by gray scale table setting



9.1.15 Enable Linear Gray Scale Table (B9h)

This command reloads the preset linear gray scale table as PW1 = 1, PW2 = 3, PW3 = 5, …., PW62 = 123, PW63 = 125 DCLKs.

9.1.16 Set V_{PA}, V_{PB} and V_{PC} Voltage for Color A, B and C (BBh, BCh and BDh)

These three commands are used to set V_{PA}, V_{PB} and V_{PC} phase 2 voltage level for color A, B and C respectively. The commands are valid in condition that these voltages are selected to generate internally by command ADh. It can be programmed to set the pre-charge voltage reference to V_{REF} or V_{COMH}.

9.1.17 Set V_{COMH} Voltage (BEh)

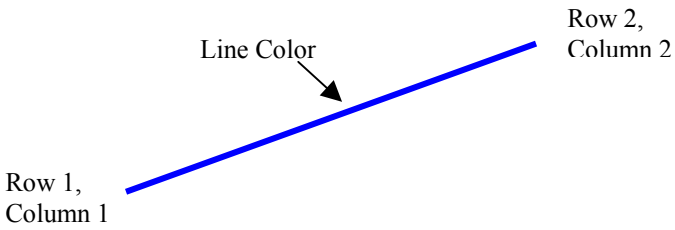
This command sets the high voltage level of common pins, V_{COMH}, when it is selected to generate internally by command ADh. The level of V_{COMH} is programmed with reference to V_{REF}.

9.2 GRAPHIC ACCELERATION COMMAND SET DESCRIPTION

9.2.1 Draw Line (21h)

This command draws a line by the given start, end column and row coordinates and the color of the line.

Figure 9-8 : Example of Draw Line Command



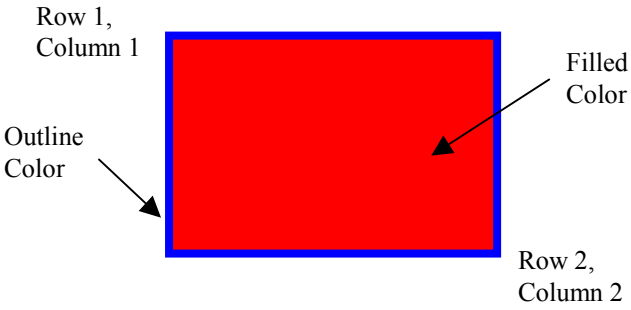
For example, the line above can be drawn by the following command sequence.

1. Enter into draw line mode by command 21h
2. Send column start address of line, column1, for example = 1h
3. Send row start address of line, row 1, for example = 10h
4. Send column end address of line, column 2, for example = 28h
5. Send row end address of line, row 2, for example = 4h
6. Send color C, B and A of line, for example = 35d, 0d, 0d for blue color

9.2.2 Draw Rectangle (22h)

Given the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2), specify the outline and fill area colors, a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.

Figure 9-9 : Example of Draw Rectangle Command



The following example illustrates the rectangle drawing command sequence.

1. Enter the “draw rectangle mode” by execute the command 22h
2. Set the starting column coordinates, Column 1. e.g., 03h.
3. Set the starting row coordinates, Row 1. e.g., 02h.
4. Set the finishing column coordinates, Column 2. e.g., 12h
5. Set the finishing row coordinates, Row 2. e.g., 15h
6. Set the outline color C, B and A. e.g., (28d, 0d, 0d) for blue color
7. Set the filled color C, B and A. e.g., (0d, 0d, 40d) for red color

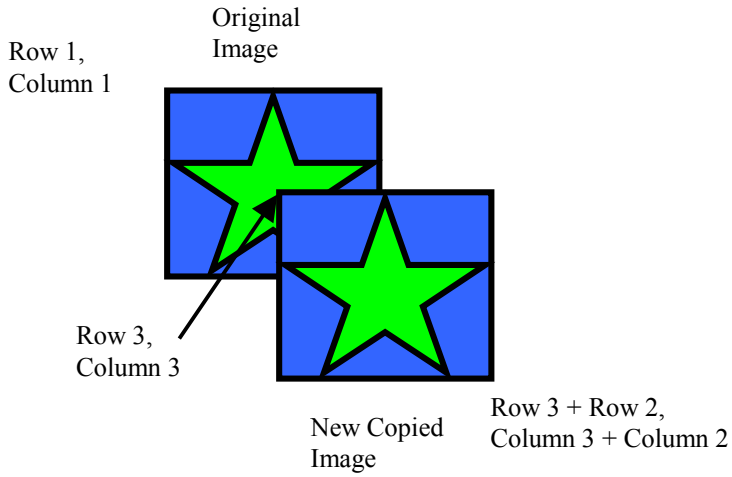
9.2.3 Copy (23h)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

1. Enter the "copy mode" by execute the command 23h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 03h
7. Set the new row coordinates, Row 3. E.g., 03h

Figure 9-10 : Example of Copy Command



9.2.4 Dim Window (24h)

This command will dim the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2). After the execution of this command, the selected window area will become darker as follow.

Table 9-1 : Result of Change of Brightness by Dim Window Command

Original gray scale	New gray scale after dim window command
GS0 ~ GS15	No change
GS16 ~ GS19	GS4
GS20 ~ GS23	GS5
:	:
GS60 ~ GS63	GS15

Additional execution of this command over the same window area will not change the data content.

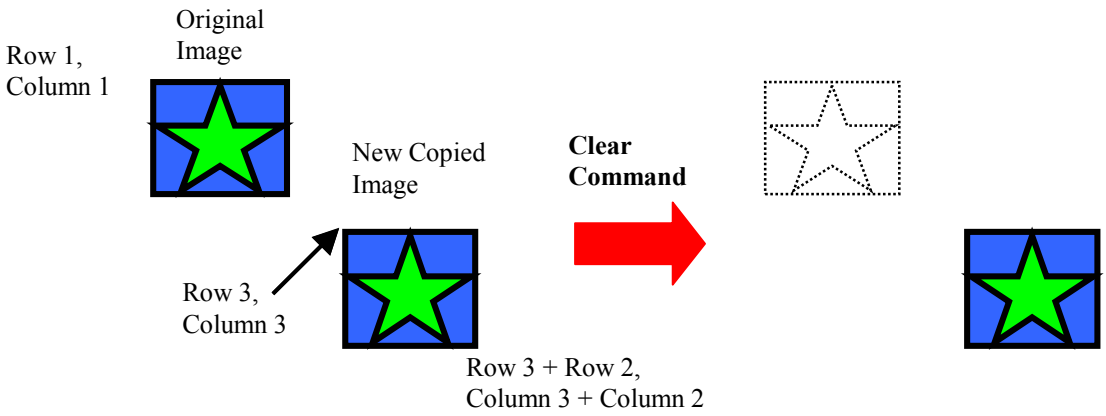
9.2.5 Clear Window (25h)

This command sets the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to clear the window display. The graphic display data RAM content of the specified window area will be set to zero.

This command can be combined with Copy command to make as a "move" result. The following example illustrates the copy plus clear procedure and results in moving the window object.

1. Enter the "copy mode" by execute the command 23h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 06h
7. Set the new row coordinates, Row 3. E.g., 06h
8. Enter the "clear mode" by execute the command 24h
9. Set the starting column coordinates, Column 1. E.g., 00h.
10. Set the starting row coordinates, Row 1. E.g., 00h.
11. Set the finishing column coordinates, Column 2. E.g., 05h
12. Set the finishing row coordinates, Row 2. E.g., 05h

Figure 9-11 : Example of Copy + Clear = Move Command



9.2.6 Fill Enable/Disable (26h)

This command has two functions.

- Enable/Disable fill (A[0])
  0 = Disable filling of color into rectangle in draw rectangle command. (POR)
  1 = Enable filling of color into rectangle in draw rectangle command.
- Enable/Disable reverse copy (A[4])
  0 = Disable reverse copy (POR)
  1 = During copy command, the new image colors are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62", ….

10 MAXIMUM RATINGS

Table 10-1 : Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 18	V
V_{REF}		0 to 18	V
V_{COMH}	Supply Voltage/Output voltage	0 to 16	V
-	SEG/COM output voltage	0 to 16	V
V_{in}	Input voltage	Vss-0.3 to Vdd+0.3	V
T_A	Operating Temperature	-40 to +90	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

11 DC CHARACTERISTICS

Table 11-1 : DC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage		7	11	18	V
V_{DD}	Logic Supply Voltage		2.4	2.7	3.5	V
V_{OH}	High Logic Output Level	Iout =100uA, 3.3MHz	0.9*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	Iout =100uA, 3.3MHz	0	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	Iout =100uA, 3.3MHz	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	Iout =100uA, 3.3MHz	0	-	0.2*V_{DD}	V
I_{SLEEP}	Sleep mode Current	VDD=2.7V, Display OFF, No panel attached	-	-	5	uA
I_{CC}	Vcc Supply Current	V_{DD}=2.7V, VCC=11V, Display ON Contrast =FF, No panel attached	-	770	-	uA
I_{DD}	V_{DD} Supply Current	V_{DD}=2.7V, VCC=11V, Display ON Contrast =FF, No panel attached	-	170	-	uA
I_{SEG}	Segment Output Current Setting V_{DD}=2.7V, V_{CC}=11V, I_{REF}=10uA, All one pattern, Display on, Segment pin under test is connected with a 33KΩ resistive load to Vcc.	Contrast = FF	-	160	-	uA
		Contrast = AF		110		uA
		Contrast = 5F	-	60	-	uA
		Contrast = 00	-	0	-	uA
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:287] = Segment current at contrast = FF	-	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-	±2.0	--	%
Vcc	Booster output voltage (Vcc)	Vin=3V, L=22uH; R1=450Kohm; R2=50Kohm; Icc = 30mA(soaking)	11	-	13	V
Pwr	Booster output power	Vin=3V, L=22uH; Vcc = 10 V ~ 16V	-	-	400	mW

12 AC CHARACTERISTICS

Table 12-1 : AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.7V	-	0.97	-	MHz
F_{FRM}	Frame Frequency for 64 MUX Mode	96RGB x 64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} X 1/(D*K*64) (2)	-	Hz

Note

(1) FOSC stands for the frequency value of the internal oscillator

(2) D: divide ratio (POR=1)
K: number of display clocks (POR=136, i.e. phase1 dclk+phase2 dclk+ phase3 dclk=4+7+125)

Table 12-2 : I²C Interface Timing Characteristics

(V_{DD}-V_{SS}=2.4 to 3.5V, T_A=-40 to 90° C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Figure 12-1 : I²C interface characteristics

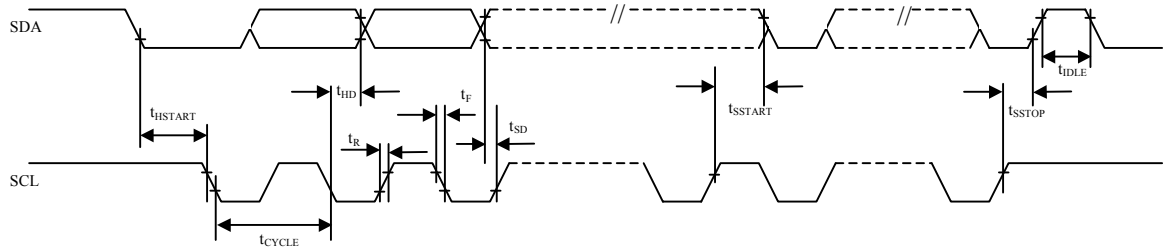


Table 12-3 : 6800-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -40 to 90°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 12-2 : 6800-series MPU parallel interface characteristics

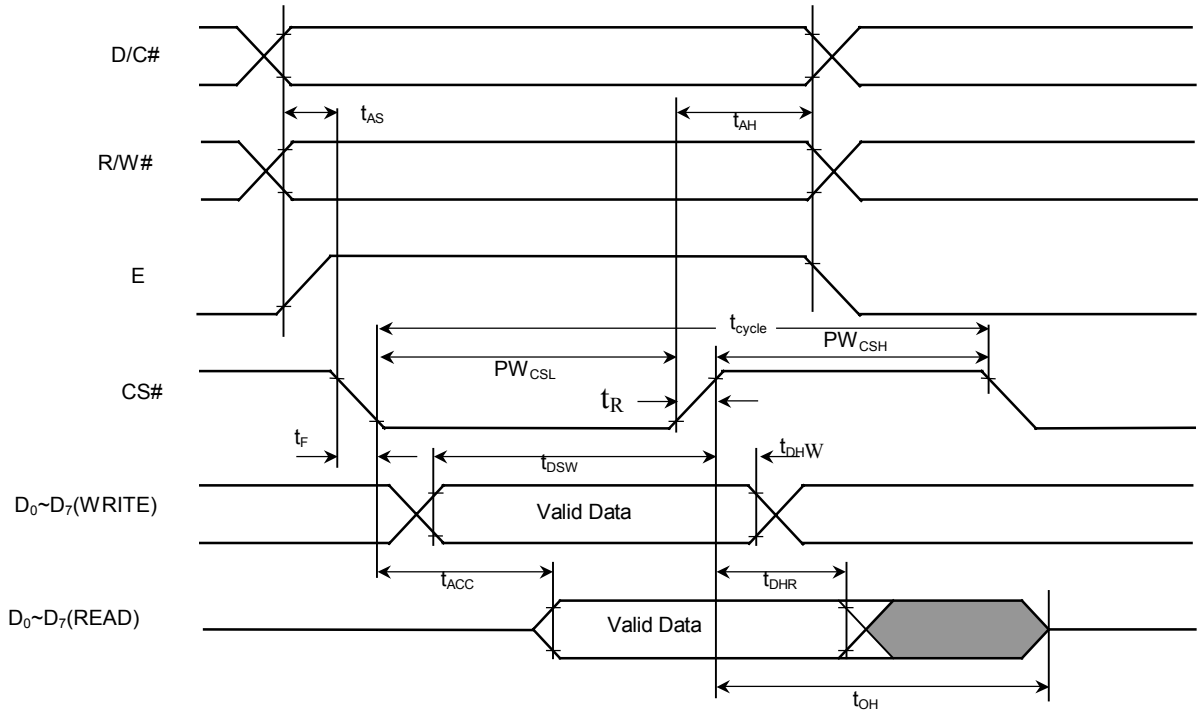


Table 12-4 : 8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -40 to 90°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 12-3 : 8080-series MPU parallel interface characteristics

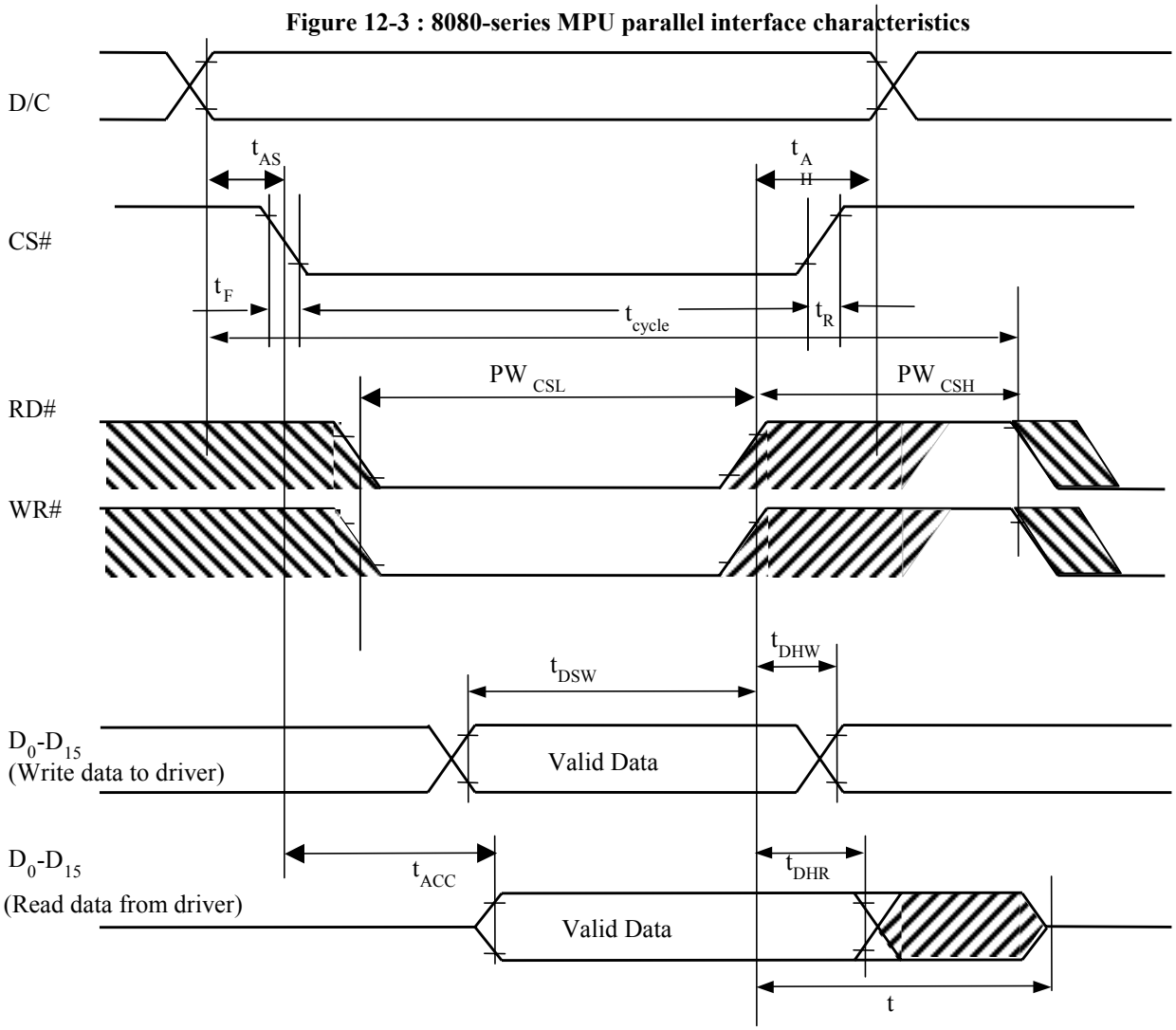
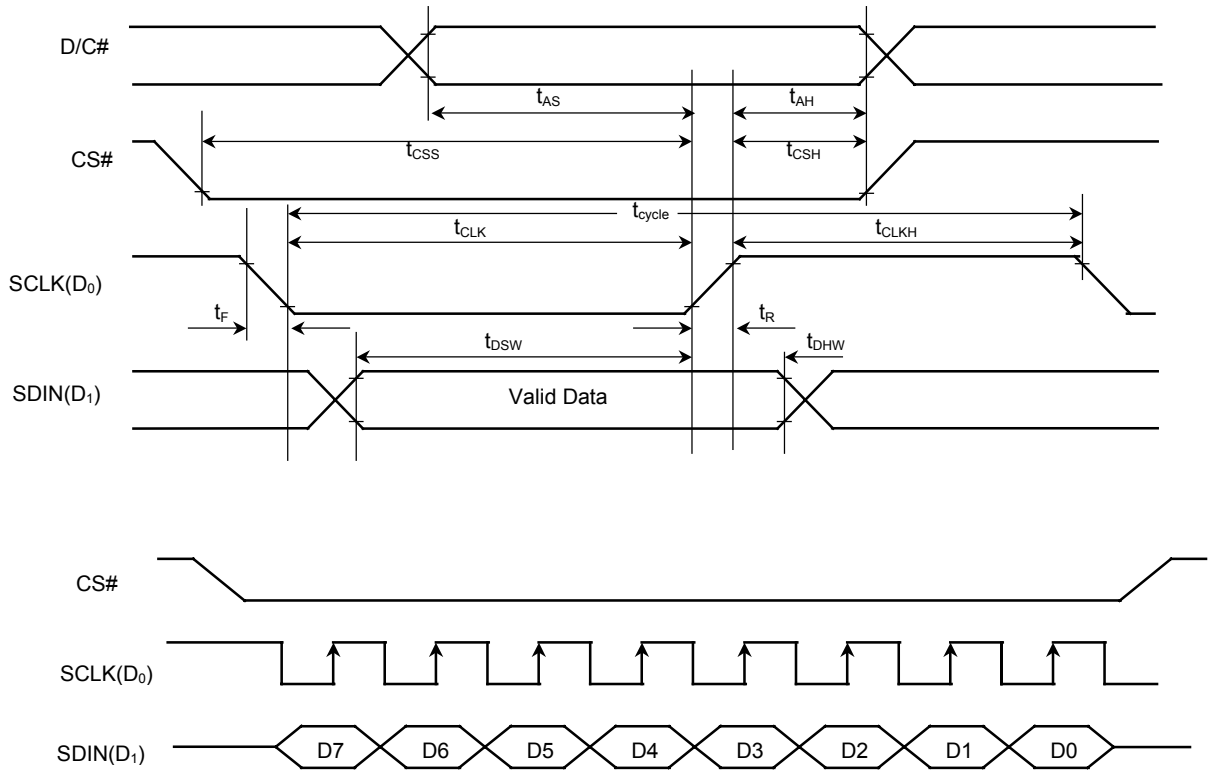


Table 12-5 : Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -40 to 90°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 12-4 : Serial interface characteristics



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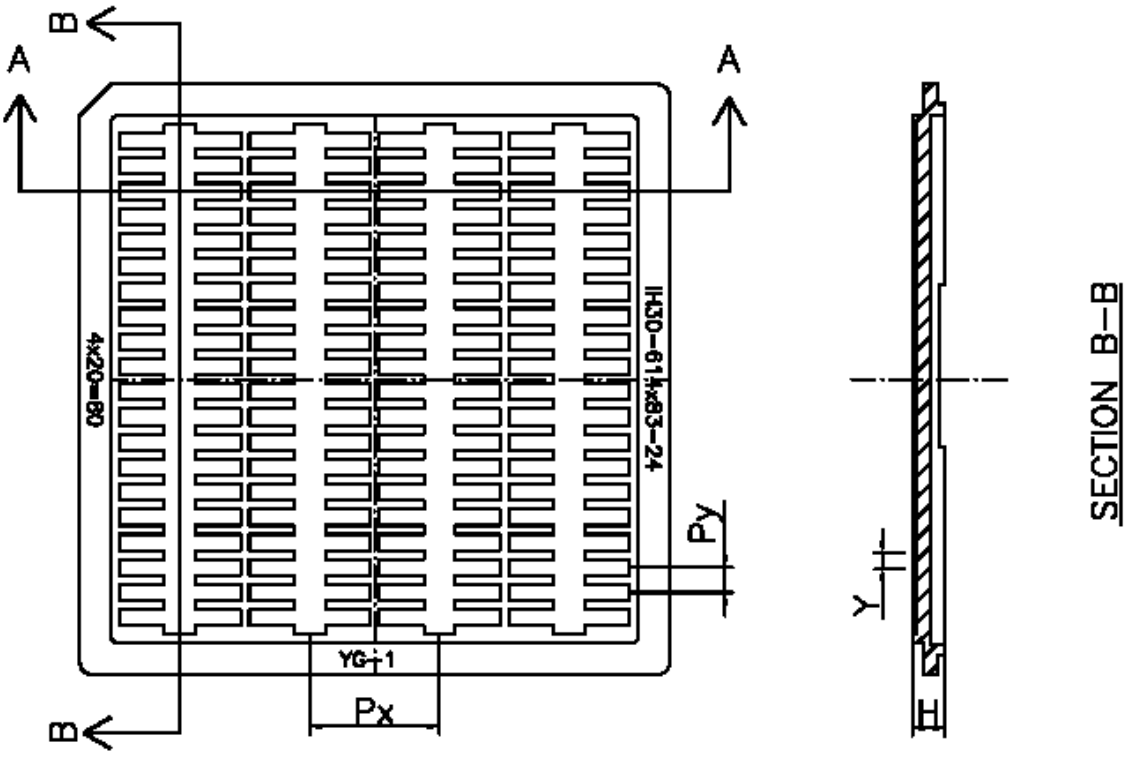

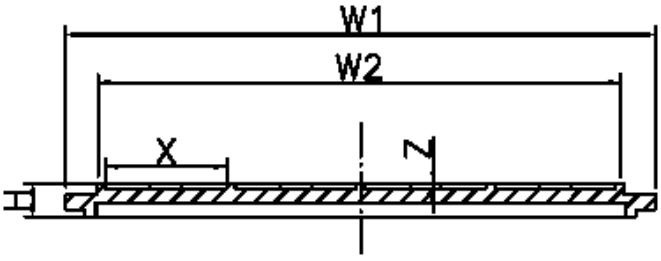

SECTION A–A

	Spec	
	mm	(mil)
W1	76.0 +0.2/-0.1	(2992)
W2	68.0 +0.2/-0.1	(2677)
H	4.20 +/-0.1	(165)
Px	20.36 +/-0.1	(802)
Py	3.23 +/-0.1	(127)
X	15.60 +/-	(614)
Y	2.10 +/-	(83)
Z	0.61 +/-0.05	(24)
N	80	