

# **SSD1325**

## ***Advance Information***

**128 x 80, 16 Gray Scale Dot Matrix  
OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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## GENERAL DESCRIPTION

The SSD1325 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 208 high voltage/current driving output pins for driving 128 segments and 80 commons. This IC is designed for Common Cathode type OLED/PLED panel.

The SSD1325 displays data directly from its internal 128x80x4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

It has a 128-step contrast control and a 16 gray level control. The embedded on-chip oscillator and DC-DC voltage converter reduce the number of external components.

## FEATURES

- Support max. 128 x 80 matrix panel
- Power supply: VDD=2.4V - 3.5V  
VCC=8.0V - 16.0V
- OLED driving output voltage, 14V maximum
- DC-DC voltage converter
- Segment maximum source current: 300uA
- Common maximum sink current: 40mA
- Embedded 128 x 80 x 4 bit SRAM display memory
- External current reference
- 128 step contrast control on monochrome passive OLED panel
- 16 gray scale
- On-Chip Oscillator
- Programmable Frame Rate
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Row re-mapping and Column re-mapping
- Low power consumption (<5.0uA @sleep mode)
- Wide range of operating temperature: -40 to 85 °C

## ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference
SSD1325Z	128	80	COG	Page 7
SSD1325T3R1	96	64	TAB	Page 36
SSD1325UR1	96	64	COF	Page 32
SSD1325U2	128	64	Punched COF	Page 40

# BLOCK DIAGRAM

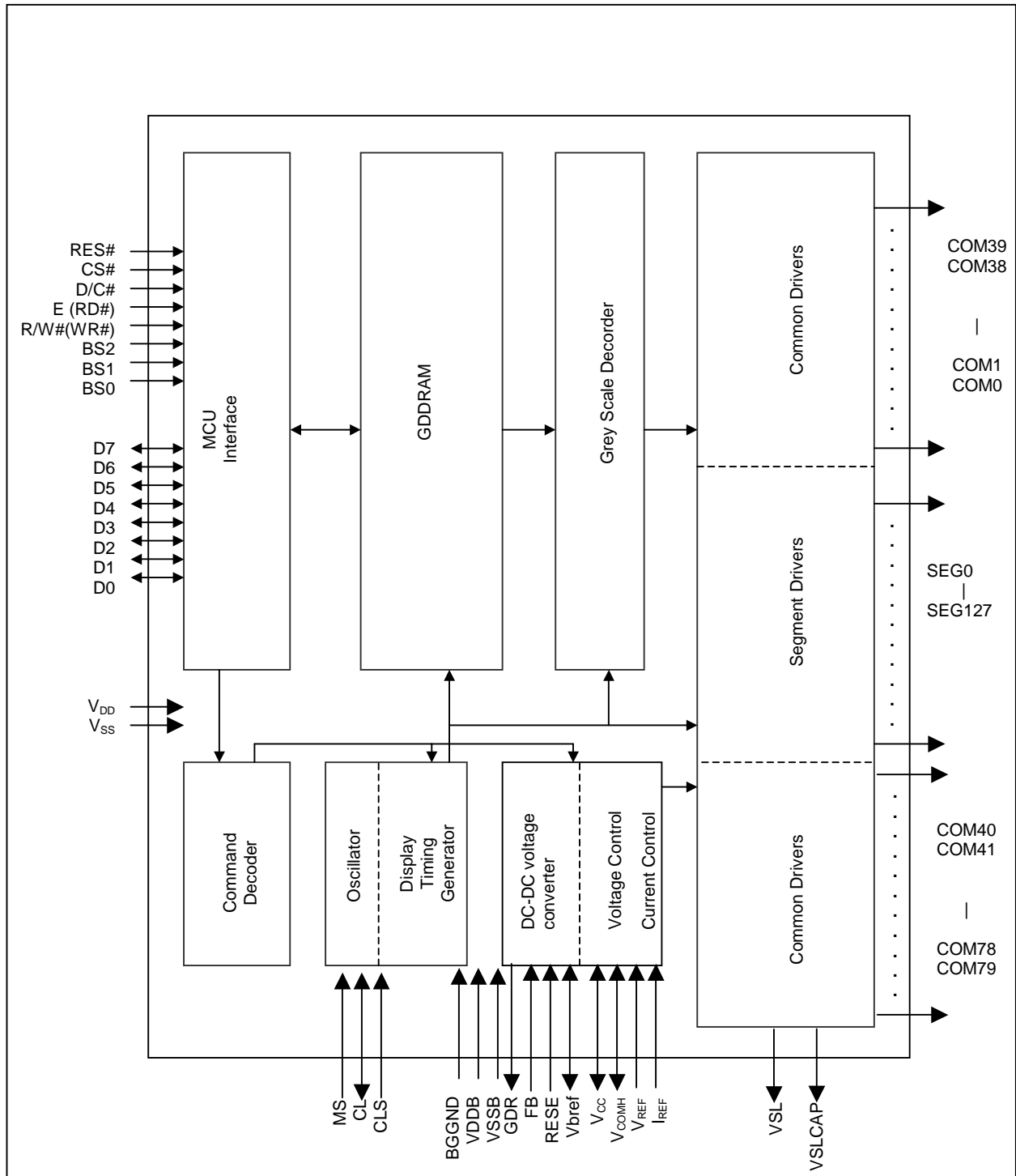


Figure 1 - Block Diagram







## PIN DESCRIPTION

### **M, DOF#**

These pins are No Connection pins. Nothing should be connected to these pins, nor they are connected together. These pins should be left open individually.

### **CL**

This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. In this case, the output clock frequency equals to the internal clock frequency. When internal oscillator is disabled, this pin receives display clock signal from external clock source.

### **M/S#**

This pin is an input pin and must be pulled high to enable the chip function.

### **CLS**

This pin is internal clock enable. When this pin is pulled high, internal clock is enabled. The internal clock will be disabled when it is pulled low, an external clock source must be connected to CL pin for normal operation.

### **BS0, BS1, BS2**

These pins are MCU interface selection input. See the following table:

Table 3 - MCU interface setting

	6800-parallel interface	8080-parallel interface	Serial interface
BS0	0	0	0
BS1	0	1	0
BS2	1	1	0

### **CS#**

This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

### **RES#**

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

### **D/C#**

This pin is Data/Command control pin. When the pin is pulled high, the input at D<sub>7</sub>-D<sub>0</sub> is treated as display data. When the pin is pulled low, the input at D<sub>7</sub>-D<sub>0</sub> will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

### **R/W# (WR#)**

This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "LOW" for write mode. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.

**E (RD#)**

This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.

**D<sub>7</sub>-D<sub>0</sub>**

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D<sub>1</sub> will be the serial data input SDIN and D<sub>0</sub> will be the serial clock input SCLK.

**V<sub>DD</sub>**

This is a voltage supply pin. It must be connected to external source.

**V<sub>SS</sub>**

This is a ground pin. It also acts as a reference for the logic pins and the OLED driving voltages. It must be connected to external ground.

**V<sub>CC</sub>**

This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC-DC voltage converter.

**V<sub>REF</sub>**

This pin is the voltage reference for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can be either supplied externally or connected to V<sub>CC</sub>.

**I<sub>REF</sub>**

This pin is segment current reference pin. A resistor should be connected between this pin and V<sub>SS</sub>. Set the current at 10uA.

**V<sub>COMH</sub>**

This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When V<sub>COMH</sub> is generated internally, a capacitor should be connected between this pin and V<sub>SS</sub>.

**VSL**

This pin is the output pin for the voltage output low level for SEG signals. A capacitor should be connected between this pin and V<sub>SS</sub>.

**VSLCAP**

This pin is the output pin for the voltage output low level for SEG signals. A capacitor should be connected between this pin and V<sub>SS</sub>.

**VCL**

This pin is the output pin for the voltage output low level for COM signals. This pin should be connected to V<sub>SS</sub>.

**VDDB**

This is the power supply pin for the GDR pin buffer. It must be connected when the converter is used.

**VSSB**

This is the GND pin for the GDR pin buffer. It must be connected when the converter is used.

**GDR**

This output pin drives the gate of the external NMOS of the booster circuit.

**FB**

This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level ( $V_{cc}$ ).

**RESE**

This pin connects to the source current pin of the external NMOS of the booster circuit.

 **$VB_{REF}$** 

This pin is the internal voltage reference of booster circuit. A stabilization capacitor should be connected between this pin and  $V_{ss}$  for both internal and external  $V_{CC}$  usage.

**COM0-COM79**

These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off.

**SEG0-SEG127**

These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off.

**NC**

These pins should be left open individually.

## FUNCTIONAL BLOCK DESCRIPTIONS

### Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is high, the input at D<sub>7</sub>-D<sub>0</sub> is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D<sub>7</sub>-D<sub>0</sub> is interpreted as a Command which will be decoded and be written to the corresponding command register.

### MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D<sub>7</sub>-D<sub>0</sub>), R/W#(WR#), D/C#, E (RD#), CS#. R/W#(WR#) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W# (WR#) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C# input. The E (RD#) input serves as data latch signal (clock) when high provided that CS# is low. Refer to Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3 below.

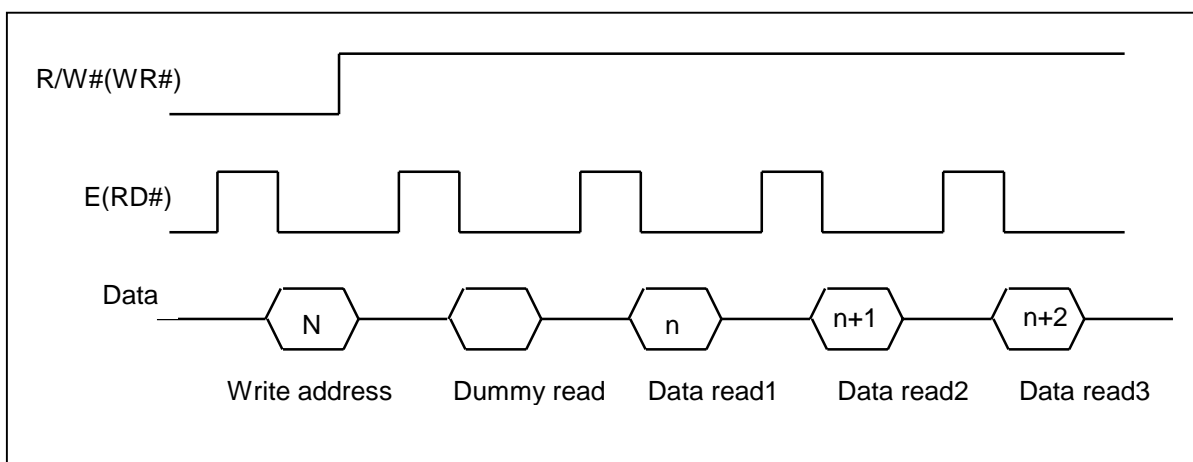


Figure 3 - Display Data Read Back Procedure - Insertion of Dummy Read

### MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D<sub>7</sub>-D<sub>0</sub>), E (RD#), R/W#(WR#), D/C#, CS#. The E (RD#) input serves as data read latch signal (clock) when it is low, and provided that CS# is low. Data read latch signal is disable when E (RD#) is high. Display data or status register read is controlled by D/C#. R/W# (WR#) input serves as data write latch signal (clock) when it is low and provided that CS# is low. Display data or command register write is controlled by D/C#. Refer to Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

### MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D<sub>7</sub>, D<sub>6</sub>, ... D<sub>0</sub>. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

## Oscillator Circuit and Display Time Generator

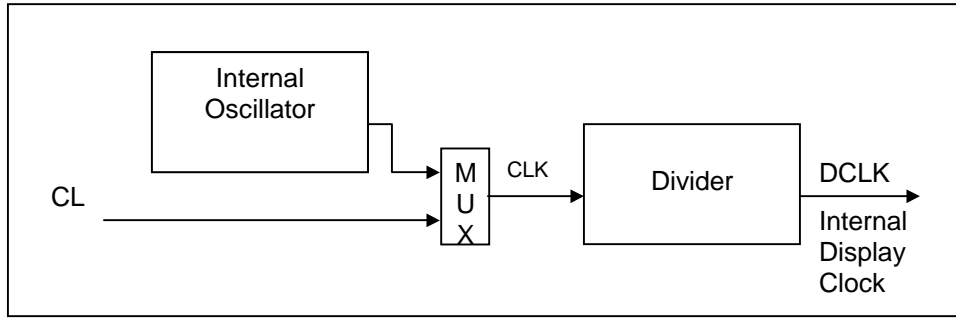


Figure 4 - Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the Display Timing Generator.

### Current Control and Voltage Control

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.  $V_{CC}$  and  $V_{DD}$  are external power supplies.  $V_{REF}$  is reference voltage, which is used to derive driving voltage for segments and commons.  $I_{REF}$  is a reference current source for segment current drivers.

### Segment Drivers/Common Drivers

Segment drivers deliver 128 current sources to drive OLED panel. The driving current can be adjusted from 0 to 300uA with 128 steps. Common drivers generate voltage scanning pulse.

### Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to Table 3-7 for GDDRAM address map description)

Table 4 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs Row Address (HEX)  
(Display Startline=0)

**Table 5 – GDDRAM address map showing Horizontal Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM Outputs	Row Address (HEX)	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]	(HEX)
COM0	00										
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
COM78	4E										
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	

(Display Startline=0)

**Table 6 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		3F		3E			01		00		Column Address
COM Outputs	Row Address (HEX)	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	(HEX)
COM0	00										
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
COM78	4E										
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]	

(Display Startline=0)

**Table 7 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM Outputs	Row Address (HEX)	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	(HEX)
COM15	0F										
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM17	11										
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

(Display Startline=10H)

**Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, ... , D5118, D5119)**

**Table 8 – GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, ... , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00										
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										
COM Outputs	Row Address (HEX)										

(Display Startline=0)

### Gray Scale Decoder

There are 16 gray levels from GS0 to GS15. The gray scale of the display is defined by the pulse width (PW) of current drive phase, GS0 has no pre-charge and no current drive. Each L value represents an offset to the corresponding gray scale level. See below table and graphical representation:

**Table9 - Gray scale pulse width set table**

	Description	Number of DCLKs
L1	Set GS1 level Pulse Width	0-7
L2	Set GS2 level Pulse Width Offset	1-8
L3	Set GS3 level Pulse Width Offset	1-8
.	.	.
.	.	.
.	.	.
L13	Set GS13 level Pulse Width Offset	1-8
L14	Set GS14 level Pulse Width Offset	1-8
L15	Set GS15 level Pulse Width Offset	1-8

DCLK: Internal Display Clock. It is used for defining phase clock period.

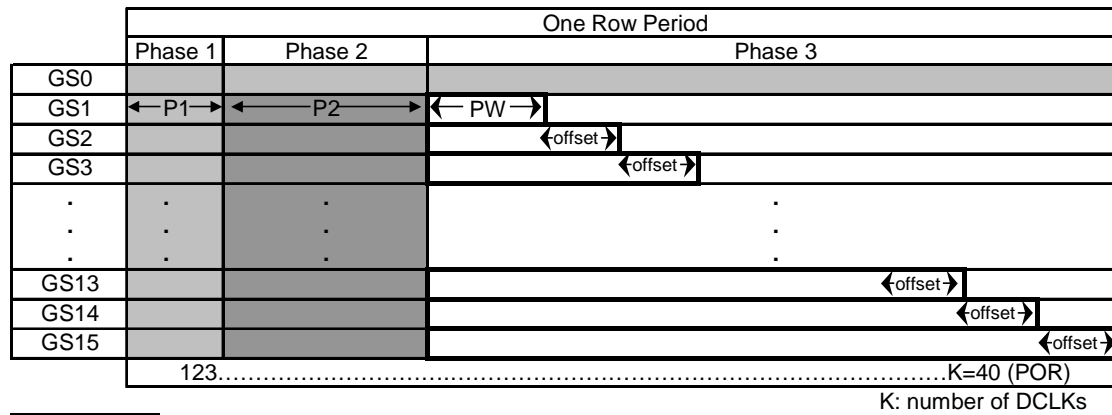


Figure 5 - Gray scale pulse width set diagram

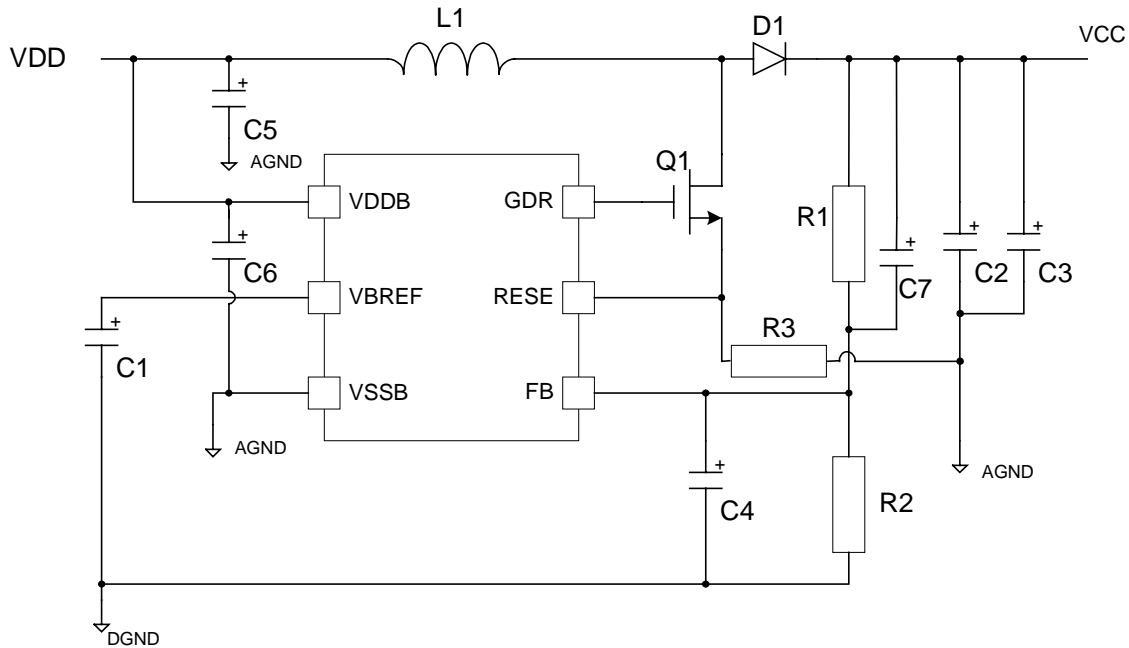
Table 10 - Gray scale pulse width default values

POR	Result
L1=1	GS1 level Pulse width=1
L2=1	GS2 level Pulse width=3
L3=1	GS3 level Pulse width=5
L4=1	GS4 level Pulse width=7
L5=1	GS5 level Pulse width=9
L6=1	GS6 level Pulse width=11
L7=1	GS7 level Pulse width=13
L8=1	GS8 level Pulse width=15
L9=1	GS9 level Pulse width=17
L10=1	GS10 level Pulse width=19
L11=1	GS11 level Pulse width=21
L12=1	GS12 level Pulse width=23
L13=1	GS13 level Pulse width=25
L14=1	GS14 level Pulse width=27
L15=1	GS15 level Pulse width=29



## DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for handheld applications. In SSD1325, internal DC-DC voltage converter accompanying with an external application circuit (shown in below figure) can generate a high voltage supply  $V_{CC}$  from a low voltage supply input  $V_{DD}$ .  $V_{CC}$  is the voltage supply to the OLED driver block. Below application circuit is an example for the input voltage of 3V  $V_{DD}$  to generate  $V_{CC}$  of 12V @20mA ~ 30mA application.



Remark:

1. L1, D1, Q1, C5 should be grouped closed together on PCB layout.
2. R1, R2, C1, C4 should be grouped closed together on PCB layout.
3. The  $V_{CC}$  output voltage level can be adjusted by R1 and R2, the reference formula is:  

$$V_{CC} = 1.2 \times (R1+R2) / R2$$
 The value of  $(R1+R2)$  should be between 500k to 1M Ohm.

Table 11 - Passive component selection:

Components	Typical Value	Remark
L1	Inductor, 22 $\mu$ H	2A
D1	Schottky diode	2A, 25V e.g. 1N5822
Q1	MOSFET	N-FET with low $R_{DS(on)}$ and low $V_{th}$ voltage. e.g. MGSF1N02LT1 [ON SEMICONDUCTOR]
R1, R2	Resistor	1%, 1/10W
R3	Resistor, 1.5 $\Omega$	1%, 1/2W
C1	Capacitor, 1 $\mu$ F	16V
C2	Capacitor, 22 $\mu$ F	Low ESR, 25V
C3	Capacitor, 1 $\mu$ F	16V
C4	Capacitor, 10nF	16V
C5	Capacitor, 1 ~ 10 $\mu$ F	16V
C6	Capacitor, 0.1 ~ 1 $\mu$ F	16V
C7	Capacitor, 15nF	16V

## COMMAND TABLE

Table 12 - Command Table

(D/C# =0, R/W#(WR#)=0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	15 A[5:0] B[5:0]	0 * *	0 * *	0 A <sub>5</sub> B <sub>5</sub>	1 A <sub>4</sub> B <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub>	1 A <sub>2</sub> B <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub>	Set Column Address	Second command A[5:0] sets the column start address from 0-63, POR = 00H.  Third command B[5:0] sets the column end address from 0-63, POR = 3FH.
0 0 0	75 A[6:0] B[6:0]	0 * *	1 A <sub>6</sub> B <sub>6</sub>	1 A <sub>5</sub> B <sub>5</sub>	1 A <sub>4</sub> B <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub>	1 A <sub>2</sub> B <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub>	Set Row address	Second command A[6:0]sets the row start address from 0-79, POR = 00H.  Third command B[6:0] sets the row end address from 0-79, POR = 4FH.
0 0	81 A[6:0]	1 *	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Contrast Control Register	Double byte command to select 1 out of 128 contrast steps. Contrast increases as level increase. The level is set to 40H after POR
0	84~86	1	0	0	0	0	1	X <sub>1</sub>	X <sub>0</sub>	Set Current Range	84H = Quarter Current Range (POR) 85H = Half Current Range 86H = Full Current Range
0 0	A0 A[6:0]	1 *	0 A <sub>6</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Re-map	A[0]=0, Disable Column Address Re-map (POR) A[0]=1, Enable Column Address Re-map A[1]=0, Disable Nibble Re-map (POR) A[1]=1, Enable Nibble Re-map A[2]=0, Horizontal Address Increment (POR) A[2]=1, Vertical Address Increment A[4]=0, Disable COM Re-map disable (POR) A[4]=1, Enable COM Re-map A[5]=0, Reserved (POR) A[5]=1, Reserved A[6]=0, Disable COM Split Odd Even (POR) A[6]=1, Enable COM Split Odd Even
0 0	A1 A[6:0]	1 *	0 A <sub>6</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Start Line	Set display RAM display start line register from 0-79.  Display start line register is reset to 00H after POR.
0 0	A2 A[6:0]	1 *	0 A <sub>6</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	0 A <sub>0</sub>	Set Display Offset	Set vertical scroll by COM from 0-79.  The value is reset to 00H after POR.
0	A4~A7	1	0	1	0	0	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Display Mode	A4H = Normal Display (POR) A5H = Entire Display On, all pixels turns on in GS level 15  A6H = Entire Display Off, all pixels turns off A7H = Inverse Display

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	A8 A[6:0]	1 *	0 A <sub>6</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX, POR=4FH(80MUX)
0 0	AD A[1:0]	1 *	0 *	1 *	0 *	1 *	1 *	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Master Configuration	A[0] = 0, Disable DC-DC converter A[0] = 1, Enable DC-DC converter (POR) A[1] = 0, Disable internal VCOMH A[1] = 1, Enable internal VCOMH (POR)
0	AE~AF	1	0	1	0	X <sub>3</sub>	1	1	1	Set Display On/Off	AEH = Display Off (Sleep mode) (POR)  AFH = Display On
0 0	BE A[5:0]	1 *	0 *	1 A <sub>5</sub>	1 A <sub>4</sub>	1 A <sub>3</sub>	1 A <sub>2</sub>	1 A <sub>1</sub>	0 A <sub>0</sub>	Set VCOMH Voltage	Second command A[5:0] sets the VCOMH voltage level 000000-011111  A[5:0] = 1xxxxx = 1.0*VREF A[5:0] = 010001(POR)
0 0	BC A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	1 A <sub>5</sub>	1 A <sub>4</sub>	1 A <sub>3</sub>	1 A <sub>2</sub>	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Precharge Voltage	Second command A[7:0] sets the precharge voltage level 00000000-00011111  A[7:0] = 1xxxxxxx connects to VCOMH A[7:0] = 001xxxxx equals 1.0*VREF A[7:0] = 00011000(POR)
0 0 0	B1 A[3:0] A[7:4]	1 * A <sub>7</sub>	0 * A <sub>6</sub>	1 * A <sub>5</sub>	1 * A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLK clocks, POR = 3DLKS = 3H  A[7:4] = P2, phase 2 period of 1-15 DCLK clocks, POR = 5DLKS = 5H
0 0	B2 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	1 A <sub>5</sub>	1 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	0 A <sub>0</sub>	Set Row Period	The next command sets the number of DCLKs, K, per row between 2-158DLKS, POR = 37DLKS = 25H  The K value should be set as K = P1+P2+GS15 pulse width (POR: 3+5+29DLKS)
0 0 0	B3 A[3:0] A[7:4]	1 * A <sub>7</sub>	0 * A <sub>6</sub>	1 * A <sub>5</sub>	1 * A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Clock Divide Ratio/Oscillator Frequency	The lower nibble of the next command sets the divide ratio of the display clocks: Divide ratio = 1-16, POR = 2  The higher nibble of the next command sets the Oscillator Frequency. Oscillator Frequency increases with the value of  A[7:4] and vice versa. POR=0

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next eight bytes of command set the gray scale level of GS1-15 as below:  A[2:0] = L1, POR=1 B[2:0] = L2, POR=1 B[6:4] = L3, POR=1 C[2:0] = L4, POR=1 C[6:4] = L5, POR=1 D[2:0] = L6, POR=1 D[6:4] = L7, POR=1 E[2:0] = L8, POR=1 E[6:4] = L9, POR=1 F[2:0] = L10, POR=1 F[6:4] = L11, POR=1 G[2:0] = L12, POR=1 G[6:4] = L13, POR=1 H[2:0] = L14, POR=1 H[6:4] = L15, POR=1
0	A[2:0]	*	*	*	*	*	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	B[2:0]	*	*	*	*	*	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	B[6:4]	*	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	*	*	*	*		
0	C[2:0]	*	*	*	*	*	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
0	C[6:4]	*	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	*	*	*	*		
0	D[2:0]	*	*	*	*	*	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		
0	D[6:4]	*	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	*	*	*	*		
0	E[2:0]	*	*	*	*	*	E <sub>2</sub>	E <sub>1</sub>	E <sub>0</sub>		
0	E[6:4]	*	E <sub>6</sub>	E <sub>5</sub>	E <sub>4</sub>	*	*	*	*		
0	F[2:0]	*	*	*	*	*	F <sub>2</sub>	F <sub>1</sub>	F <sub>0</sub>		
0	F[6:4]	*	F <sub>6</sub>	F <sub>5</sub>	F <sub>4</sub>	*	*	*	*		
0	G[2:0]	*	*	*	*	*	G <sub>2</sub>	G <sub>1</sub>	G <sub>0</sub>		
0	G[6:4]	*	G <sub>6</sub>	G <sub>5</sub>	G <sub>4</sub>	*	*	*	*		
0	H[2:0]	*	*	*	*	*	H <sub>2</sub>	H <sub>1</sub>	H <sub>0</sub>		
0	H[6:4]	*	H <sub>6</sub>	H <sub>5</sub>	H <sub>4</sub>	*	*	*	*		
0	CF	1	1	0	0	1	1	1	1	Set Biasing Current for DC-DC converter	FOH = High (POR) 70H = Low
0	A[7:6]	A <sub>7</sub>	A <sub>6</sub>	*	*	*	*	*	*		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

**Table 13 - Read Command Table**

(D/C#=0, R/W#(WR#)=1, E(RD#)=1 for 6800 or E(RD#)=0 for 8080)

D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	Status Register Read	D7 = 0:reserved D7 = 1:reserved D6 = 0:indicates the display is ON D6 = 1:indicated the display is OFF D5 = 0:reserved D5 = 1:reserved D4 = 0:reserved D4 = 1:reserved
---	----------------------	---

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; Otherwise, unexpected result will occur

**Data Read / Write**

To read data from the GDDRAM, input High to R/W# (WR#) pin and D/C# pin for 6800-series parallel mode, Low to E (RD#) pin and High to D/C# pin for 8080-series parallel mode.

In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data read. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/W#(WR#) pin and High to D/C# pin for 6800-series parallel mode and 8080-series parallel mode. For serial interface mode, it is always in write mode. In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data write. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data write.

It should be noted that, in horizontal address increment mode, the row address pointer would be increased by one automatically if the column address pointer wraps around. In vertical address increment mode, the column address pointer will be increased by one automatically if the row address pointer wraps around.

**Table 14 - Address Increment Table (Automatic)**

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

## COMMAND DESCRIPTIONS

### Set Column Address

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address.

### Set Row Address

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address.

### Set Contrast Control Register

This command is to set Contrast Setting of the display. The chip has 128 contrast steps from 00H to 7FH. The segment output current increases linearly with the increase of contrast step. See Figure 6 below.

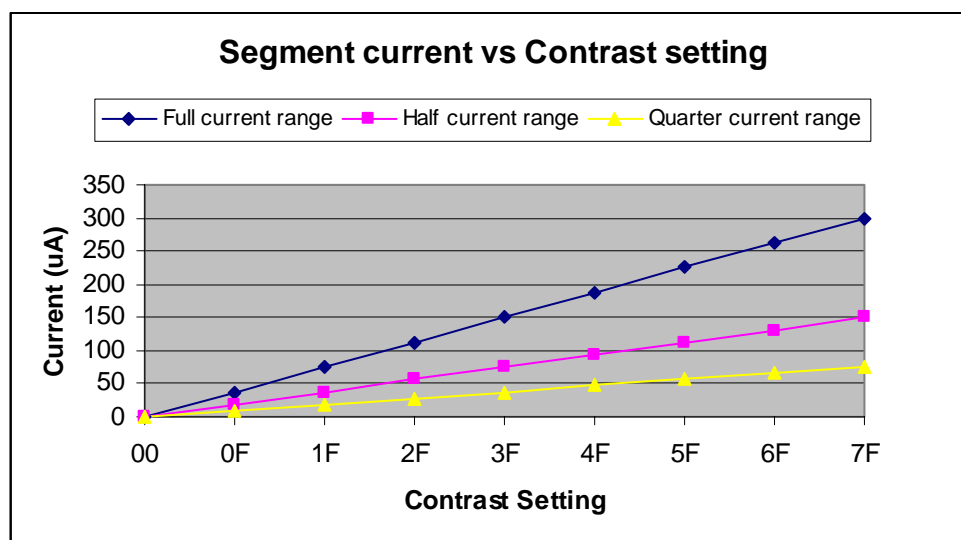


Figure 6 - Segment current vs Contrast setting

### Set Current Range

This command is used to select quarter range or half range or full range current mode. With the same contrast level, quarter range mode will give a quarter of the current output of the full range mode. Similar to half range current mode, it will give a half of the current output of the full range mode. See Figure 6. In POR, quarter range current mode is default.

### Set Re-map

This command changes the mapping between the display data column address and segment driver, row address and common driver. It allows flexibility in layout during OLED module assembly. See the Re-map setting below:

#### Column Address Re-map

If column address re-map is set, Col 0-63 map to SEG127-0, regardless of start column and end column commands.

#### Nibble Re-map

If nibble re-map is set, the two nibbles of the data bus for RAM access are re-mapped, such that (D7, D6, D5, D4, D3, D2, D1, D0) acts like (D3, D2, D1, D0, D7, D6, D5, D4)

This feature working with Column Address Re-map would produce an effect of flipping outputs SEG0-127 to SEG127-SEG0.

#### Address Increment Mode

If horizontal increment mode is set, the column address pointer advances after each RAM access.

If vertical increment mode is set, the row address pointer advances after each RAM access.

#### COM Re-map

If COM re-map is set, ROW 0-79 map to COM79-0, regardless of start and end row commands.

### **Set Display Start Line**

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 79.

### **Set Display Offset**

This is a double byte command. The next command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-79.

For example, to move the COMX towards the COM0 direction for L lines, the 7-bit data in the second command should be given by L. In other words, to move the COMX towards the COM79 direction for L lines, the 7-bit data in the second command should be given by 80-L.

### **Set Display Mode**

This command is used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display. Set Entire Display On forces the entire display to be at gray level "GS15" regardless of the contents of the display data RAM. Set Entire Display Off forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM. Normal Display will turn the data to ON at the corresponding gray level. Inverse display will turn the data as follow:

**Table 15 - Mapping of data with each gray scale level at different display mode**

Data D <sub>x4</sub> D <sub>x3</sub> D <sub>x2</sub> D <sub>x1</sub>	Normal Display (A4H)	Entire Display On (A5H)	Entire Display Off (A6H)	Inverse Display (A7H)
0000	GS0	GS15	GS0	GS15
0001	GS1	GS15	GS0	GS14
0010	GS2	GS15	GS0	GS13
0011	GS3	GS15	GS0	GS12
0100	GS4	GS15	GS0	GS11
0101	GS5	GS15	GS0	GS10
0110	GS6	GS15	GS0	GS9
0111	GS7	GS15	GS0	GS8
1000	GS8	GS15	GS0	GS7
1001	GS9	GS15	GS0	GS6
1010	GS10	GS15	GS0	GS5
1011	GS11	GS15	GS0	GS4
1100	GS12	GS15	GS0	GS3
1101	GS13	GS15	GS0	GS2
1110	GS14	GS15	GS0	GS1
1111	GS15	GS15	GS0	GS0

### **Set Multiplex Ratio**

This command sets multiplex ratio from 16 to 80. In POR, multiplex ratio is 80.

### Set DC-DC Converter

This command is used to enable or disable the internal DC-DC voltage converter. This command will be executed when display is on.

### Set Display On/Off

This command turns the display on or off. When the display is off, the segment and common output are in high impedance state.

### Set $V_{COMH}$ Voltage

This command is used to set  $V_{COMH}$  voltage level

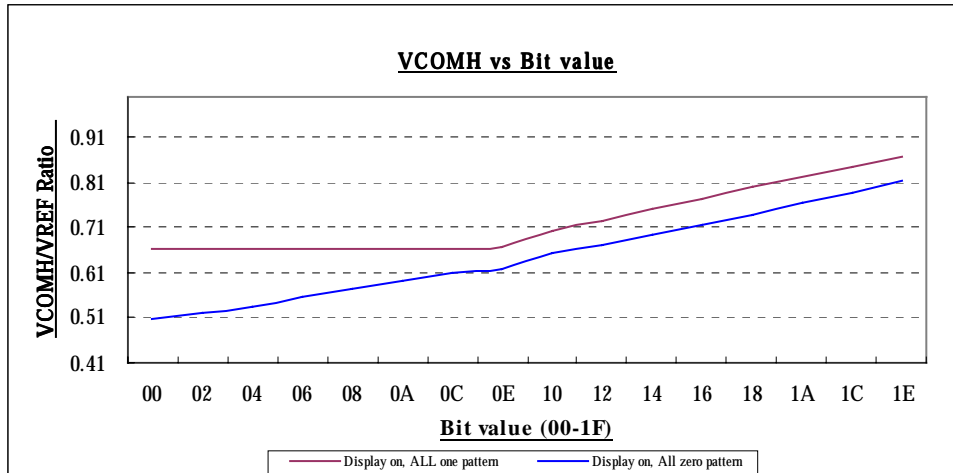


Figure 7 - VCOMH vs Bit value

### Set Precharge Voltage

This command is used to set Precharge Voltage level

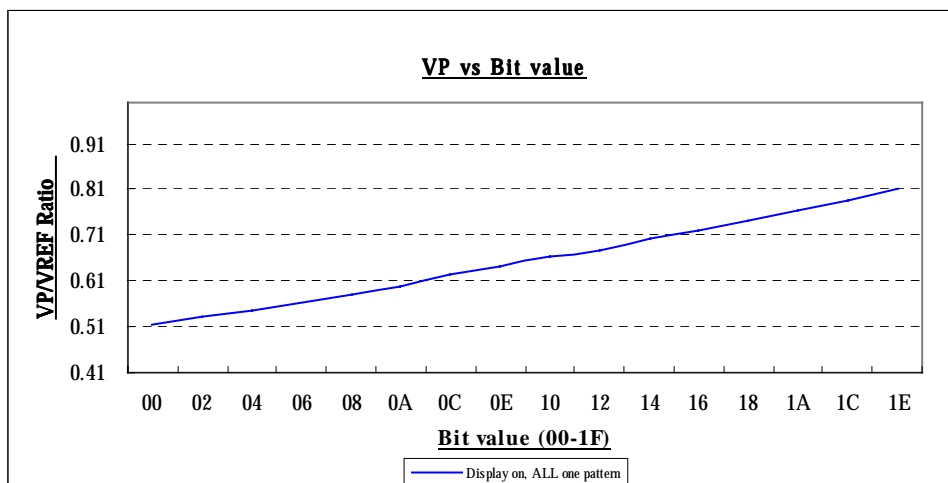


Figure 8 - VP vs Bit value



### **Set Phase Length**

This is a double byte command. The lower nibble of the second byte selects phase 1 period (no pre-charge and current drive) from 1 to 16 DCLKs. POR is A[3:0]=3d. The higher nibble of the second byte is used to select phase 2 period (pre-charge) from 1 to 16 DCLKs. POR is A[7:4]=5d.

### **Set Row Period**

This command is used to set the row period. It is defined by multiplying the internal display clock period by the number of internal display clocks per row (Value from 2-158d). POR is 37d. The larger the value, the more precise of each gray scale level can be tuned. See “Gray Scale Table” command for details. Also, It is used to define the frame frequency with the use of “Display Clock Divide Ratio” command together.

Row period equals to the sum of phase 1, 2 periods and the pulse width of GS15. See equation in command table on page 12.

### **Set Display Clock Divide Ratio**

This command is used to set the frequency of the internal display clocks, DCLKs. It is defined by dividing the oscillator frequency by the divide ratio (Value from 1 to 16). POR is 2. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency. See equation on page 12.

### **Set Oscillator Frequency**

This is a double byte command. The lower nibble of the second byte is used to select the oscillator frequency. Default value is shown in Table 12.

### **Set Gray Scale Table**

This command is used to set the gray scale table for the display. Except GS0, which has no pre-charge and current drive, each GS level is programmed by a set of offset values. As shown in Table 8, GS1 is defined with pulse width equals to the first offset value, L1, select from 0-7 internal display clocks. GS2 is defined with pulse width equals to GS1 plus the next offset value, L2, select from 1-8 internal display clocks. Similarly, the next GS level is defined with pulse width equals to its lower one GS level plus the next offset value, select from 1-8 internal display clocks. In normal operation, GS15 should take the full current drive period as its pulse width. Therefore, the row period should be set as the sum of phase 1 period, phase 2 period, and the pulse width of GS15 with the use of “Row period” command.

### **NOP**

No Operation Command.

### **Status register Read**

This command is issued by setting D/C# low during a data read (refer to Figure 9 and Figure 10 parallel interface waveform). It allows the MCU to monitor the internal status of the chip.

## MAXIMUM RATINGS

Table 16 - Maximum Ratings

(Voltage Reference to  $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.3 to +4	V
$V_{CC}$		0 to 16	V
$V_{REF}$		0 to 16	V
$V_{COMH}$	Supply Voltage/Output voltage	0 to 16	V
-	SEG/COM output voltage	0 to 16	V
$V_{in}$	Input voltage	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
$T_A$	Operating Temperature	-40 to +85	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

## DC CHARACTERISTICS

Table 17 - DC Characteristics

(Unless otherwise specified, Voltage Referenced to  $V_{SS}$ ,  $V_{DD} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$V_{CC}$	Operating Voltage	-	8	12	16	V
$V_{DD}$	Logic Supply Voltage	-	2.4	2.7	3.5	V
$V_{OH}$	High Logic Output Level	IOUT = 100uA, 3.3MHz	$0.9 \cdot V_{DD}$	-	$V_{DD}$	V
$V_{OL}$	Low Logic Output Level	IOUT = 100uA, 3.3MHz	0	-	$0.1 \cdot V_{DD}$	V
$V_{IH}$	High Logic Input Level	IOUT = 100uA, 3.3MHz	$0.8 \cdot V_{DD}$	-	$V_{DD}$	V
$V_{IL}$	Low Logic Input Level	IOUT = 100uA, 3.3MHz	0	-	$0.2 \cdot V_{DD}$	V
$I_{SLEEP}$	Sleep mode Current	No loading	-	0.2	5	uA
$I_{CC}$	$V_{CC}$ Supply Current <small><math>V_{DD}=2.7V</math>, external <math>V_{CC}=12V</math>, <math>I_{REF}=10uA</math>, Frame rate=110Hz, All one pattern, Display on, no loading</small>	Contrast = 7F	-	700	-	uA
$I_{DD}$	$V_{DD}$ Supply Current <small><math>V_{DD}=2.7V</math>, external <math>V_{CC}=12V</math>, <math>I_{REF}=10uA</math>, Frame rate=110Hz, All one pattern, Display on, no loading</small>	Contrast = 7F	-	-	650	uA
$I_{SEG}$	Segment Output Current <small><math>V_{DD}=2.7V</math>, <math>V_{CC}=12V</math>, <math>I_{REF}=10uA</math>, Frame rate=110Hz, Display on, Segment pin under test is connected with a 20K resistive load to VSS</small>	Contrast = 7F	270	300	370	uA
		Contrast = 5F	-	225	-	
		Contrast = 3F	-	150	-	
		Contrast = 1F	-	75	-	
Dev	Segment output current uniformity <small><math>V_{DD}=2.7V</math>, <math>V_{CC}=12V</math>, <math>I_{REF}=10uA</math>, Contrast=7F</small>	Adjacent pin	-	$\pm 2$	-	%
		Overall pin to pin	-	-	$\pm 3$	
$V_{CC}$	DC-DC converter output voltage	<small><math>V_{DD}</math> input=3V, L=22uH; R1=450Kohm; R2=50Kohm; <math>I_{CC} = 20mA</math>(loading)</small>	10	-	12	V
Pwr	DC-DC converter output power	<small><math>V_{DD}</math> input=3V, L=22uH; <math>V_{CC} = 12V</math></small>	-	-	400	mW

## AC CHARACTERISTICS

Table 18 - AC Characteristics

(Unless otherwise specified, Voltage Referenced to  $V_{SS}$ ,  $V_{DD} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ .)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$F_{OSC}$	Oscillation Frequency of Display Timing Generator	$V_{DD} = 2.7V$	535	630	725	kHz
$F_{FRM}$	Frame Frequency for 128 MUX Mode	128x80 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	$F_{OSC} \times 1/(D \times K \times 80)$	-	Hz

D: divide ratio

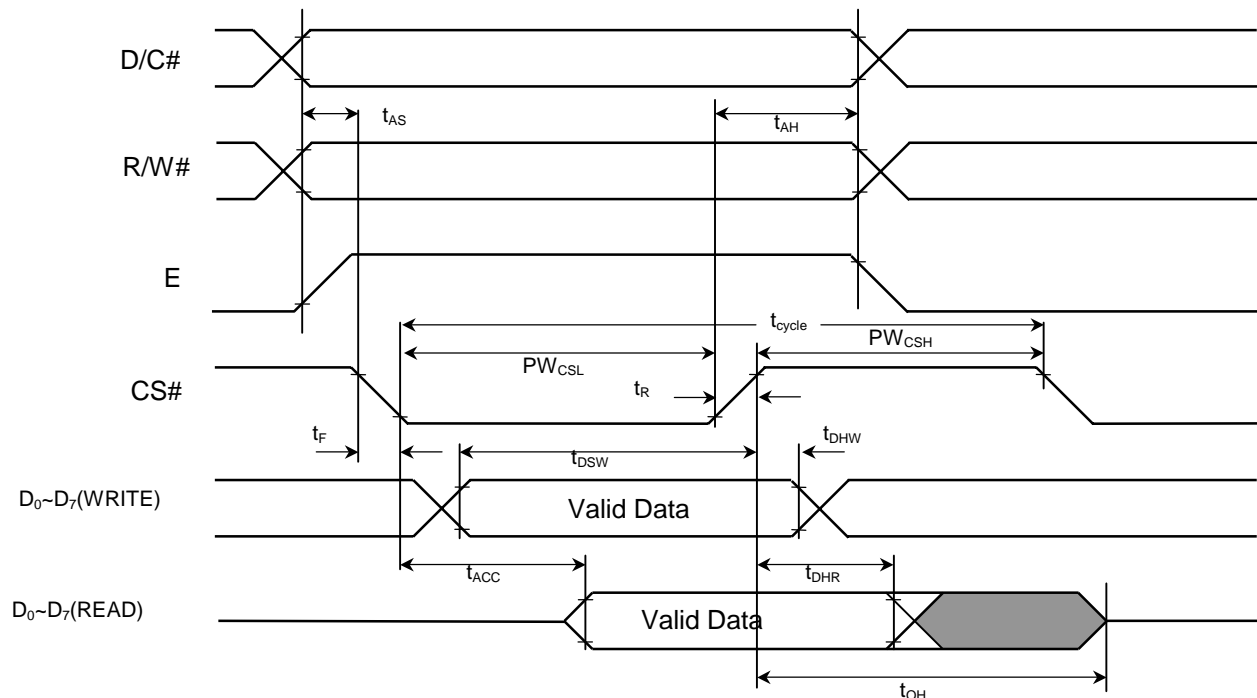
K: number of display clocks

Refer to command table for detail description

**Table 19 - 6800-Series MPU Parallel Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	0	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

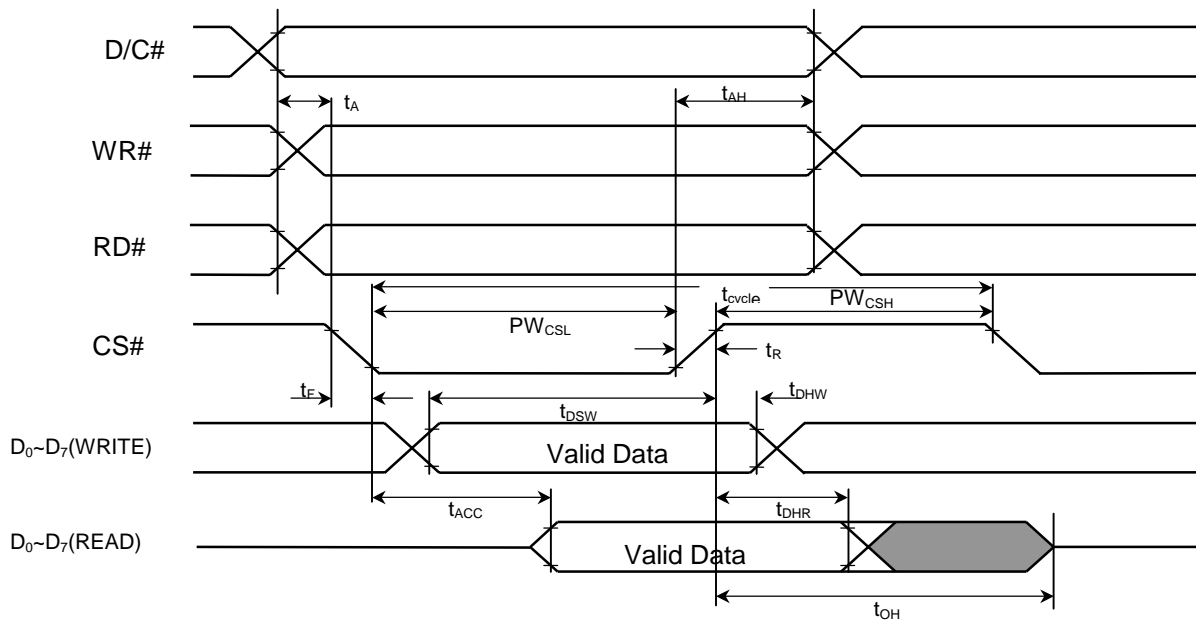


**Figure 9 - 6800-series MPU Parallel Interface Characteristics**

**Table 20 - 8080-Series MPU Parallel Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	0	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

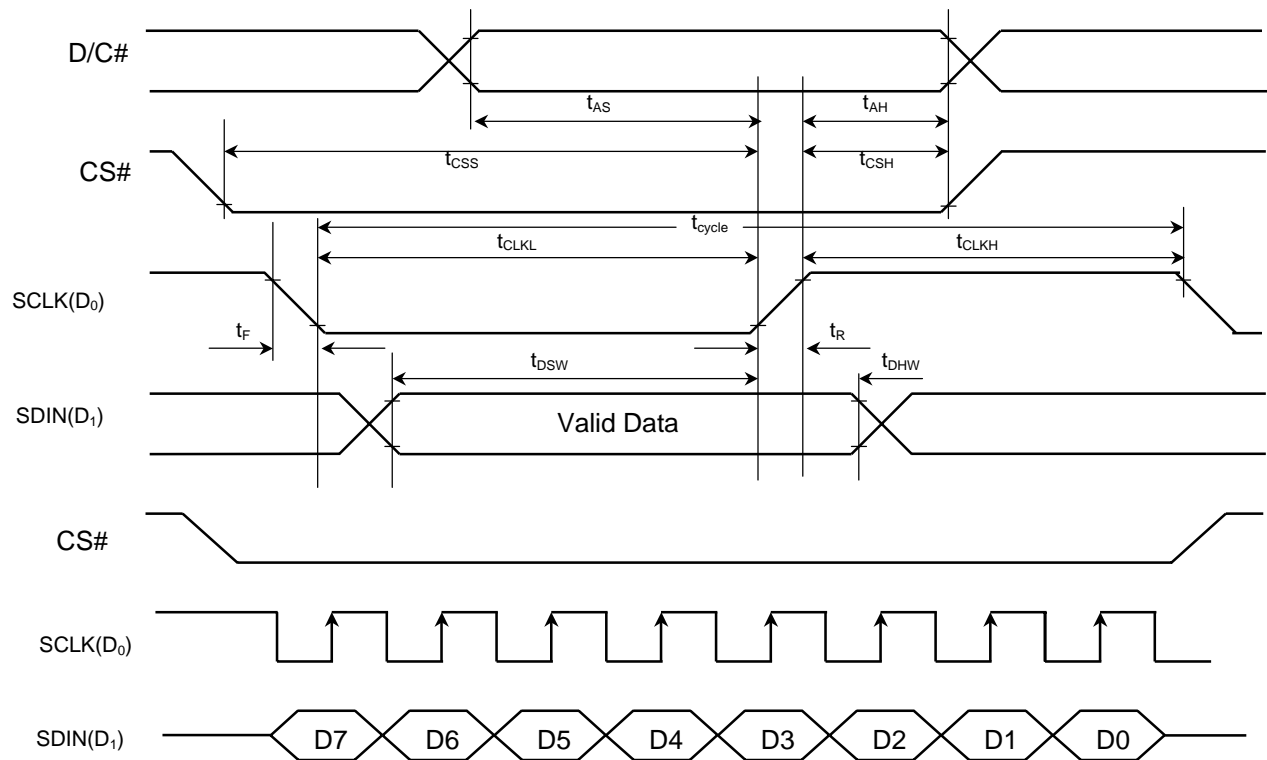


**Figure 10 - 8080-series MPU Parallel Interface Characteristics**

**Table 21 - Serial Interface Timing Characteristics**

( $V_{DD} - V_{SS} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	250	-	-	ns
$t_{AS}$	Address Setup Time	150	-	-	ns
$t_{AH}$	Address Hold Time	150	-	-	ns
$t_{CSS}$	Chip Select Setup Time	120	-	-	ns
$t_{CSH}$	Chip Select Hold Time	60	-	-	ns
$t_{DSW}$	Write Data Setup Time	100	-	-	ns
$t_{DHW}$	Write Data Hold Time	100	-	-	ns
$t_{CLKL}$	Clock Low Time	100	-	-	ns
$t_{CLKH}$	Clock High Time	100	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns



**Figure 11 - Serial Interface Characteristics**

## SSD1325Z DIE TRAY DIMENSIONS

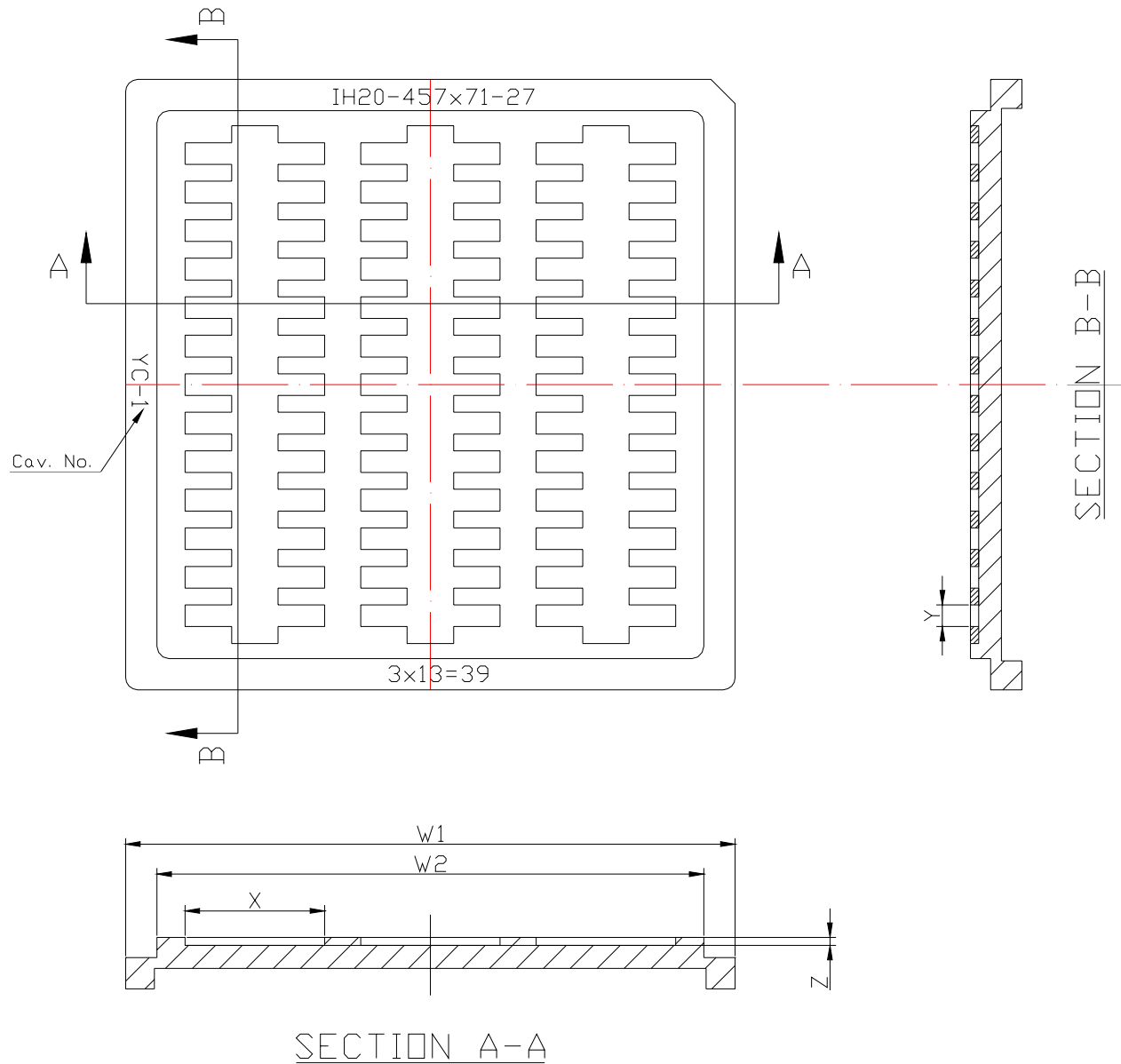


Figure 12 - SSD1325Z Die Tray Drawing

Table 22 - SSD1325Z Die Tray Dimensions

Parameter	Dimensions
W1	50.70±0.2 mm
W2	45.50±0.2 mm
X	11.60±0.1 mm
Y	1.80±0.1 mm
Z	0.71±0.05 mm
N (number of die)	39

# SSD1325UR1 PACKAGE DETAILS

## SSD1325UR1 Pin Assignment

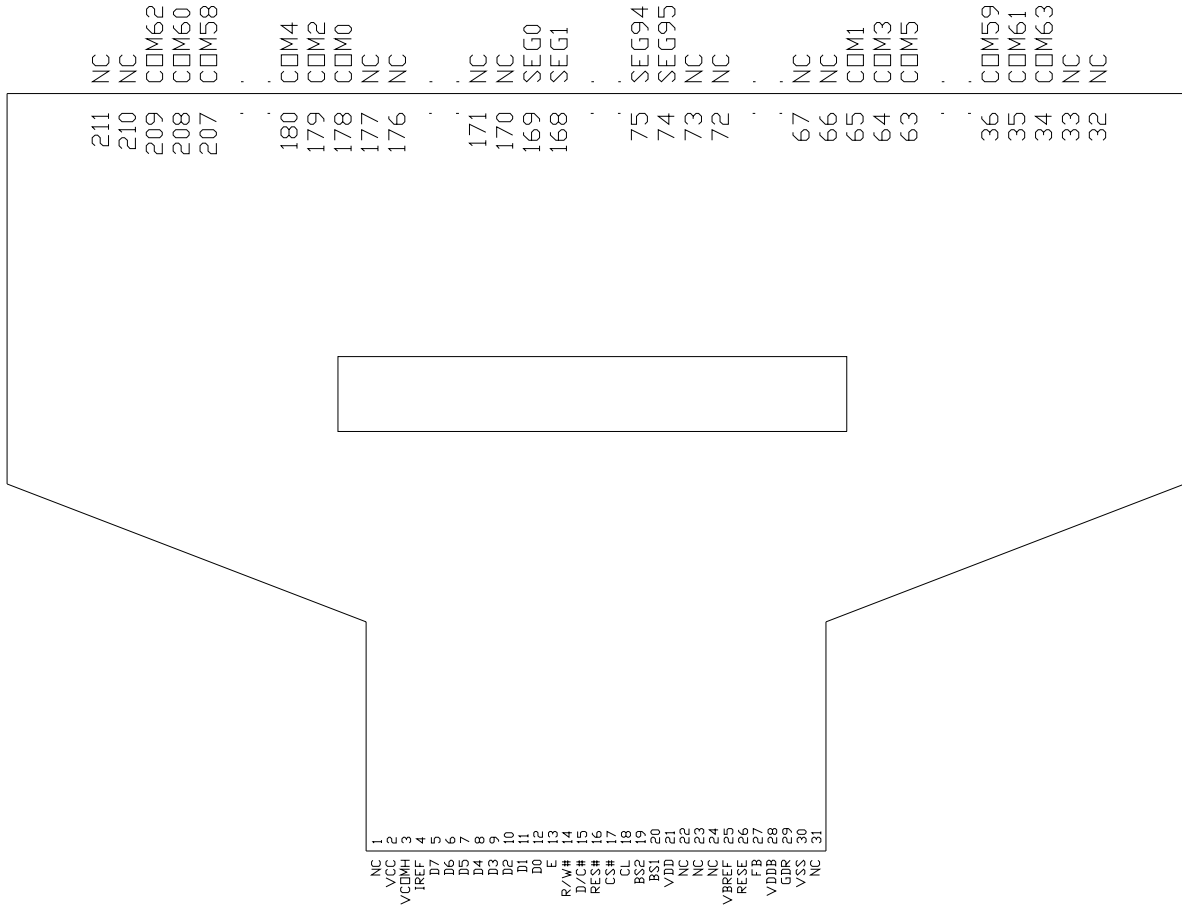


Figure 13 - SSD1325UR1 pin assignment (Copper view, Mirror COF design)

**Remark:**

1. Use internal clock
2. VREF connect to VCC
3. VSSB, BGGND connect to VSS
4. BS0 connect to VSS
5. Support 6800, 8080, and SPI modes

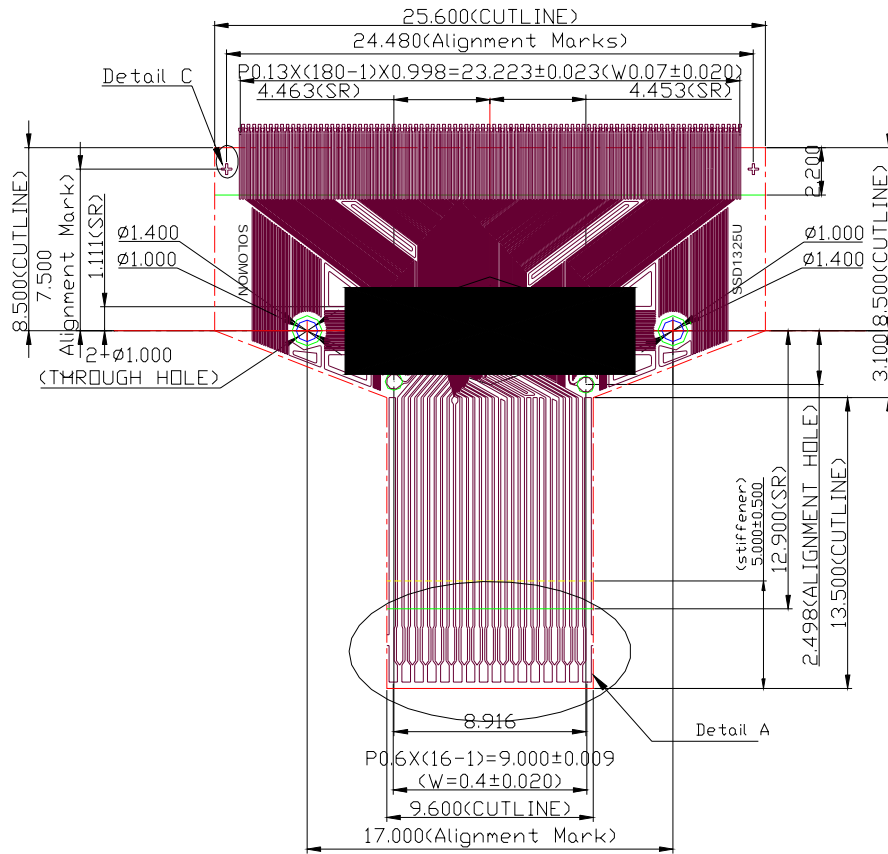


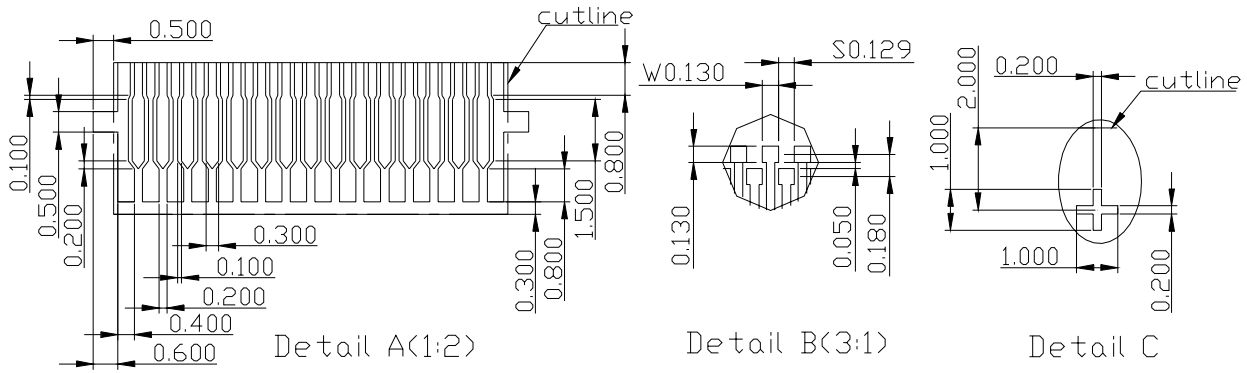
Table 23 - SSD1325UR1 pin assignment (enabled COM odd-even in "Set Re-map" command)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NC	61	COM 9	121	SEG 48	181	COM 6
2	VCC	62	COM 7	122	SEG 47	182	COM 8
3	VCOMH	63	COM 5	123	SEG 46	183	COM 10
4	IREF	64	COM 3	124	SEG 45	184	COM 12
5	D7	65	COM 1	125	SEG 44	185	COM 14
6	D6	66	NC	126	SEG 43	186	COM 16
7	D5	67	NC	127	SEG 42	187	COM 18
8	D4	68	NC	128	SEG 41	188	COM 20
9	D3	69	NC	129	SEG 40	189	COM 22
10	D2	70	NC	130	SEG 39	190	COM 24
11	D1	71	NC	131	SEG 38	191	COM 26
12	DO	72	NC	132	SEG 37	192	COM 28
13	E	73	NC	133	SEG 36	193	COM 30
14	R/W	74	SEG 95	134	SEG 35	194	COM 32
15	D/C	75	SEG 94	135	SEG 34	195	COM 34
16	RES	76	SEG 93	136	SEG 33	196	COM 36
17	CSB	77	SEG 92	137	SEG 32	197	COM 38
18	CL	78	SEG 91	138	SEG 31	198	COM 40
19	BS2	79	SEG 90	139	SEG 30	199	COM 42
20	BS1	80	SEG 89	140	SEG 29	200	COM 44
21	VDD	81	SEG 88	141	SEG 28	201	COM 46
22	NC	82	SEG 87	142	SEG 27	202	COM 48
23	NC	83	SEG 86	143	SEG 26	203	COM 50
24	NC	84	SEG 85	144	SEG 25	204	COM 52
25	VBREF	85	SEG 84	145	SEG 24	205	COM 54
26	RESE	86	SEG 83	146	SEG 23	206	COM 56
27	FB	87	SEG 82	147	SEG 22	207	COM 58
28	VDDDB	88	SEG 81	148	SEG 21	208	COM 60
29	GDR	89	SEG 80	149	SEG 20	209	COM 62
30	VSS	90	SEG 79	150	SEG 19	210	NC
31	NC	91	SEG 78	151	SEG 18	211	NC
32	NC	92	SEG 77	152	SEG 17		
33	NC	93	SEG 76	153	SEG 16		
34	COM 63	94	SEG 75	154	SEG 15		
35	COM 61	95	SEG 74	155	SEG 14		
36	COM 59	96	SEG 73	156	SEG 13		
37	COM 57	97	SEG 72	157	SEG 12		
38	COM 55	98	SEG 71	158	SEG 11		
39	COM 53	99	SEG 70	159	SEG 10		
40	COM 51	100	SEG 69	160	SEG 9		
41	COM 49	101	SEG 68	161	SEG 8		
42	COM 47	102	SEG 67	162	SEG 7		
43	COM 45	103	SEG 66	163	SEG 6		
44	COM 43	104	SEG 65	164	SEG 5		
45	COM 41	105	SEG 64	165	SEG 4		
46	COM 39	106	SEG 63	166	SEG 3		
47	COM 37	107	SEG 62	167	SEG 2		
48	COM 35	108	SEG 61	168	SEG 1		
49	COM 33	109	SEG 60	169	SEG 0		
50	COM 31	110	SEG 59	170	NC		
51	COM 29	111	SEG 58	171	NC		
52	COM 27	112	SEG 57	172	NC		
53	COM 25	113	SEG 56	173	NC		
54	COM 23	114	SEG 55	174	NC		
55	COM 21	115	SEG 54	175	NC		
56	COM 19	116	SEG 53	176	NC		
57	COM 17	117	SEG 52	177	NC		
58	COM 15	118	SEG 51	178	COM 0		
59	COM 13	119	SEG 50	179	COM 2		
60	COM 11	120	SEG 49	180	COM 4		

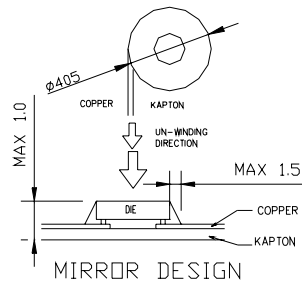
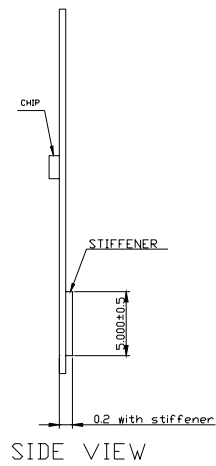
# SSD1325UR1 COF Package Dimensions

UN-WINDING  
TAPE  
DIRECTION  
↑





- NOTE:
1. GENERAL TOLERANCE:  $\pm 0.20\text{mm}$
  2. CUTLINE TOLERANCE:  $\pm 0.15\text{mm}$
  3. MATERIAL
    - PI:  $38 \pm 4\mu\text{m}$
    - CU:  $8 \pm 2\mu\text{m}$
    - SR:  $15 \pm 10\mu\text{m}$
    - OTHER TOLERANCE:  $\pm 0.200$
  4. SN PLATING:  $0.20 \pm 0.05\mu\text{m}$
  5. SOLOMON SYSTECH INTERNAL USE ONLY WHICH MAY BE REPLACED BY PUNCHING HOLE



# SSD1325T3R1 PACKAGE DETAILS

## SSD1325T3R1 Pin Assignment

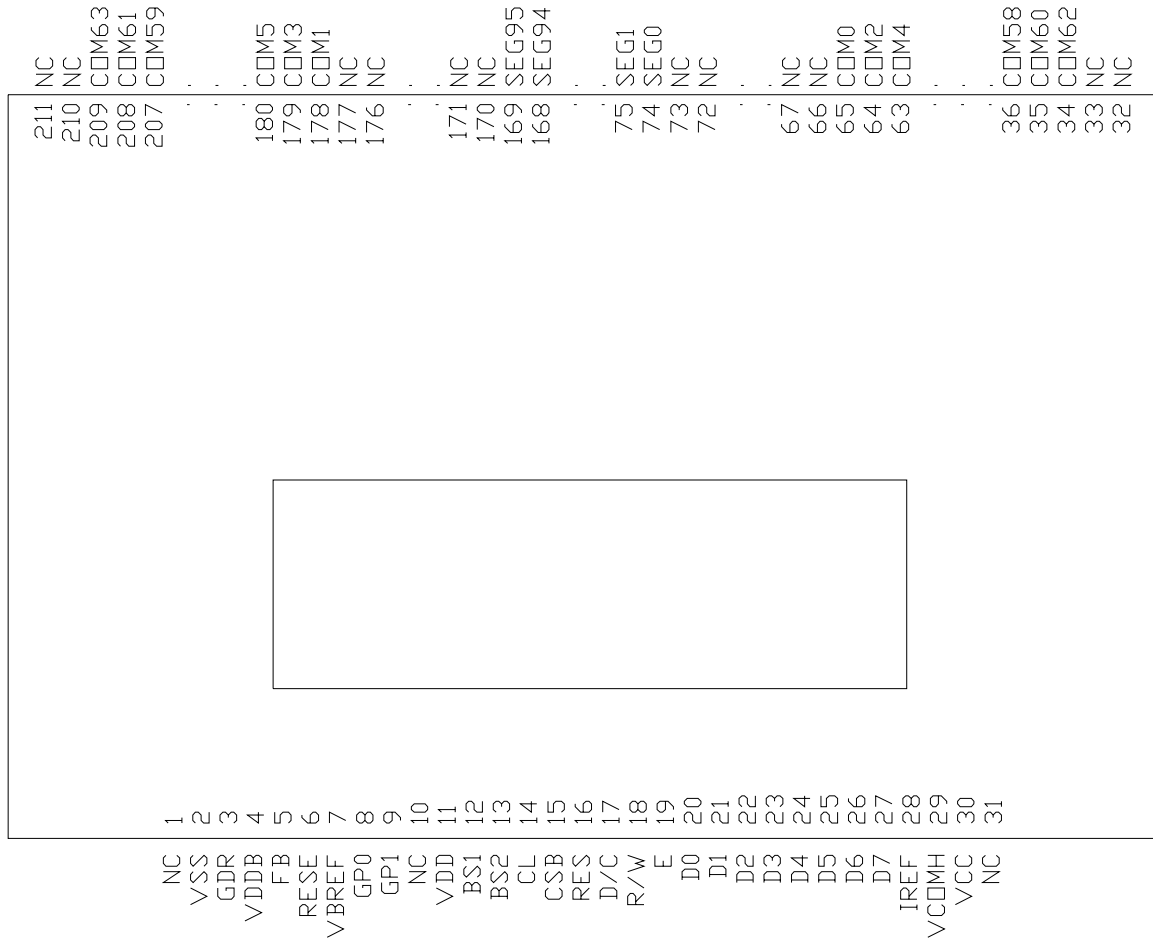


Figure 14 - SSD1325T3R1 pin assignment (Copper view, Normal TAB design)

**Remark:**

1. Use internal clock
2. VREF connect to VCC
3. VSSB, BGGND connect to VSS
4. BS0 connect to VSS
5. Support 6800, 8080, and SPI modes

Table 24 - SSD1325T3R1 pin assignment (enabled COM odd-even in "Set Re-map" command)

See next page

Pin #	Pin Name
1	NC
2	VSS
3	GDR
4	VDDB
5	FB
6	RESE
7	VBREF
8	GP0
9	GP1
10	NC
11	VDD
12	BS1
13	BS2
14	CL
15	CSB
16	RES
17	D/C
18	R/W
19	E
20	DO
21	D1
22	D2
23	D3
24	D4
25	D5
26	D6
27	D7
28	IREF
29	VCOMH
30	VCC
31	NC
32	NC
33	NC
34	COM 62
35	COM 60
36	COM 58
37	COM 56
38	COM 54
39	COM 52
40	COM 50
41	COM 48
42	COM 46
43	COM 44
44	COM 42
45	COM 40
46	COM 38
47	COM 36
48	COM 34
49	COM 32
50	COM 30
51	COM 28
52	COM 26
53	COM 24
54	COM 22
55	COM 20
56	COM 18
57	COM 16
58	COM 14
59	COM 12
60	COM 10

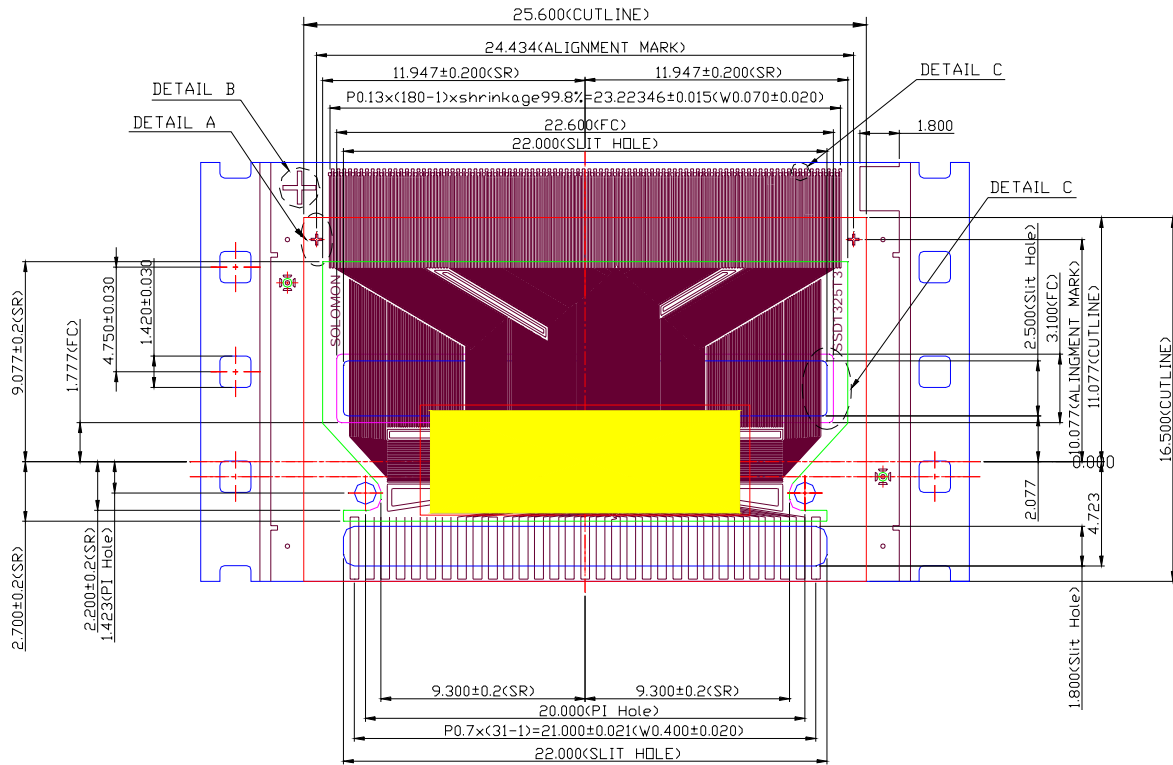
Pin #	Pin Name
61	COM 8
62	COM 6
63	COM 4
64	COM 2
65	COM 0
66	NC
67	NC
68	NC
69	NC
70	NC
71	NC
72	NC
73	NC
74	SEG 0
75	SEG 1
76	SEG 2
77	SEG 3
78	SEG 4
79	SEG 5
80	SEG 6
81	SEG 7
82	SEG 8
83	SEG 9
84	SEG 10
85	SEG 11
86	SEG 12
87	SEG 13
88	SEG 14
89	SEG 15
90	SEG 16
91	SEG 17
92	SEG 18
93	SEG 19
94	SEG 20
95	SEG 21
96	SEG 22
97	SEG 23
98	SEG 24
99	SEG 25
100	SEG 26
101	SEG 27
102	SEG 28
103	SEG 29
104	SEG 30
105	SEG 31
106	SEG 32
107	SEG 33
108	SEG 34
109	SEG 35
110	SEG 36
111	SEG 37
112	SEG 38
113	SEG 39
114	SEG 40
115	SEG 41
116	SEG 42
117	SEG 43
118	SEG 44
119	SEG 45
120	SEG 46

Pin #	Pin Name
121	SEG 47
122	SEG 48
123	SEG 49
124	SEG 50
125	SEG 51
126	SEG 52
127	SEG 53
128	SEG 54
129	SEG 55
130	SEG 56
131	SEG 57
132	SEG 58
133	SEG 59
134	SEG 60
135	SEG 61
136	SEG 62
137	SEG 63
138	SEG 64
139	SEG 65
140	SEG 66
141	SEG 67
142	SEG 68
143	SEG 69
144	SEG 70
145	SEG 71
146	SEG 72
147	SEG 73
148	SEG 74
149	SEG 75
150	SEG 76
151	SEG 77
152	SEG 78
153	SEG 79
154	SEG 80
155	SEG 81
156	SEG 82
157	SEG 83
158	SEG 84
159	SEG 85
160	SEG 86
161	SEG 87
162	SEG 88
163	SEG 89
164	SEG 90
165	SEG 91
166	SEG 92
167	SEG 93
168	SEG 94
169	SEG 95
170	NC
171	NC
172	NC
173	NC
174	NC
175	NC
176	NC
177	NC
178	COM 1
179	COM 3
180	COM 5

Pin #	Pin Name
181	COM 7
182	COM 9
183	COM 11
184	COM 13
185	COM 15
186	COM 17
187	COM 19
188	COM 21
189	COM 23
190	COM 25
191	COM 27
192	COM 29
193	COM 31
194	COM 33
195	COM 35
196	COM 37
197	COM 39
198	COM 41
199	COM 43
200	COM 45
201	COM 47
202	COM 49
203	COM 51
204	COM 53
205	COM 55
206	COM 57
207	COM 59
208	COM 61
209	COM 63
210	NC
211	NC

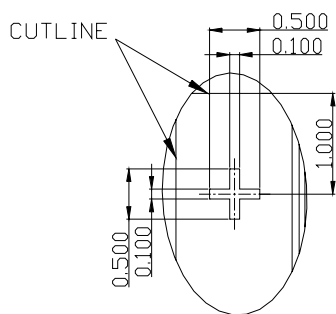
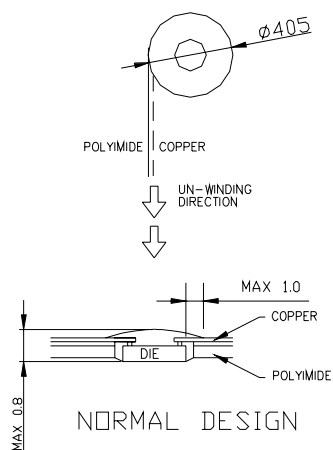
# SSD1325T3R1 TAB Package Dimensions


 TAPE  
 UN-WINDING  
 DIRECTION

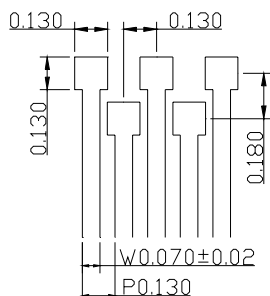


NOTE:

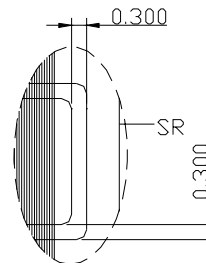
1. GENERAL TOLERANCE:  $\pm 0.05\text{mm}$
2. CUTLINE TOLERANCE:  $\pm 0.15\text{mm}$
3. MATERIAL
  - PI:  $75\pm 6\mu\text{m}$
  - CU:  $18\pm 2\mu\text{m}$
  - SR:  $26\pm 14\mu\text{m}$
4. SN PLATING:  $0.20\pm 0.05\mu\text{m}$
5. TAP SITE: 4 SPH, 19.00mm
6. SOLOMON SYSTECH INTERNAL USE ONLY WHICH MAY BE REPLACED BY PUNCHING HOLE



DETAIL A  
SCALE 2:1



DETAIL C  
SCALE 5:1



DETAIL D  
SCALE 1:1

# SSD1325U2 PACKAGE DETAILS

## SSD1325U2 Pin Assignment

1	NC	250	NC
2	NC	249	NC
3	VCC	248	CDM62
4	VCDMH	247	CDM60
5	IREF	246	CDM58
6	D7		
7	D6		
8	D5		
9	D4		
10	D3	219	CDM4
11	D2	218	CDM2
12	D1	217	CDM0
13	D0	216	NC
14	E	215	NC
15	R/W#	214	NC
16	D/C#	213	NC
17	RES#	212	NC
18	CS#	211	NC
19	NC	210	NC
20	BS2	209	NC
21	BS1	208	NC
22	VDD	207	NC
23	NC	206	NC
24	NC	205	SEG0
25	NC	204	SEG1
26	VBREF	203	SEG2
27	RESE		
28	FB		
29	VDDB	80	SEG125
30	GDR	79	SEG126
31	VSS	78	SEG127
32	NC	77	NC
		76	NC
		75	NC
		74	NC
		73	NC
		72	NC
		71	NC
		70	NC
		69	NC
		68	NC
		67	NC
		66	CDM1
		65	CDM3
		64	CDM5
		37	CDM59
		36	CDM61
		35	CDM63
		34	NC
		33	NC



Pin Name	X-Axis	Y-Axis
NC	-12.675	-6.1
VCC	-11.83	-6.1
VCOMH	-10.985	-6.1
IREF	-10.14	-6.1
D7	-9.295	-6.1
D6	-8.45	-6.1
D5	-7.605	-6.1
D4	-6.76	-6.1
D3	-5.915	-6.1
D2	-5.07	-6.1
D1	-4.225	-6.1
D0	-3.38	-6.1
E	-2.535	-6.1
RW	-1.69	-6.1
DC	-0.845	-6.1
RES	0	-6.1
CS	0.845	-6.1
NC	1.69	-6.1
BS2	2.535	-6.1
BS1	3.38	-6.1
VDD	4.225	-6.1
NC	5.07	-6.1
NC	5.915	-6.1
NC	6.76	-6.1
VBREF	7.605	-6.1
RESE	8.45	-6.1
FB	9.295	-6.1
VDDb	10.14	-6.1
GDR	10.985	-6.1
VSS	11.83	-6.1
NC	12.675	-6.1
NC	13.02	12.325
NC	12.9	12.125
COM63	12.78	12.325
COM61	12.66	12.125
COM59	12.54	12.325
COM57	12.42	12.125
COM55	12.3	12.325
COM53	12.18	12.125
COM51	12.06	12.325
COM49	11.94	12.125
COM47	11.82	12.325
COM45	11.7	12.125
COM43	11.58	12.325
COM41	11.46	12.125
COM39	11.34	12.325
COM37	11.22	12.125
COM35	11.1	12.325
COM33	10.98	12.125
COM31	10.86	12.325
COM29	10.74	12.125
COM27	10.62	12.325
COM25	10.5	12.125
COM23	10.38	12.325
COM21	10.26	12.125
COM19	10.14	12.325
COM17	10.02	12.125
COM15	9.9	12.325
COM13	9.78	12.125
COM11	9.66	12.325

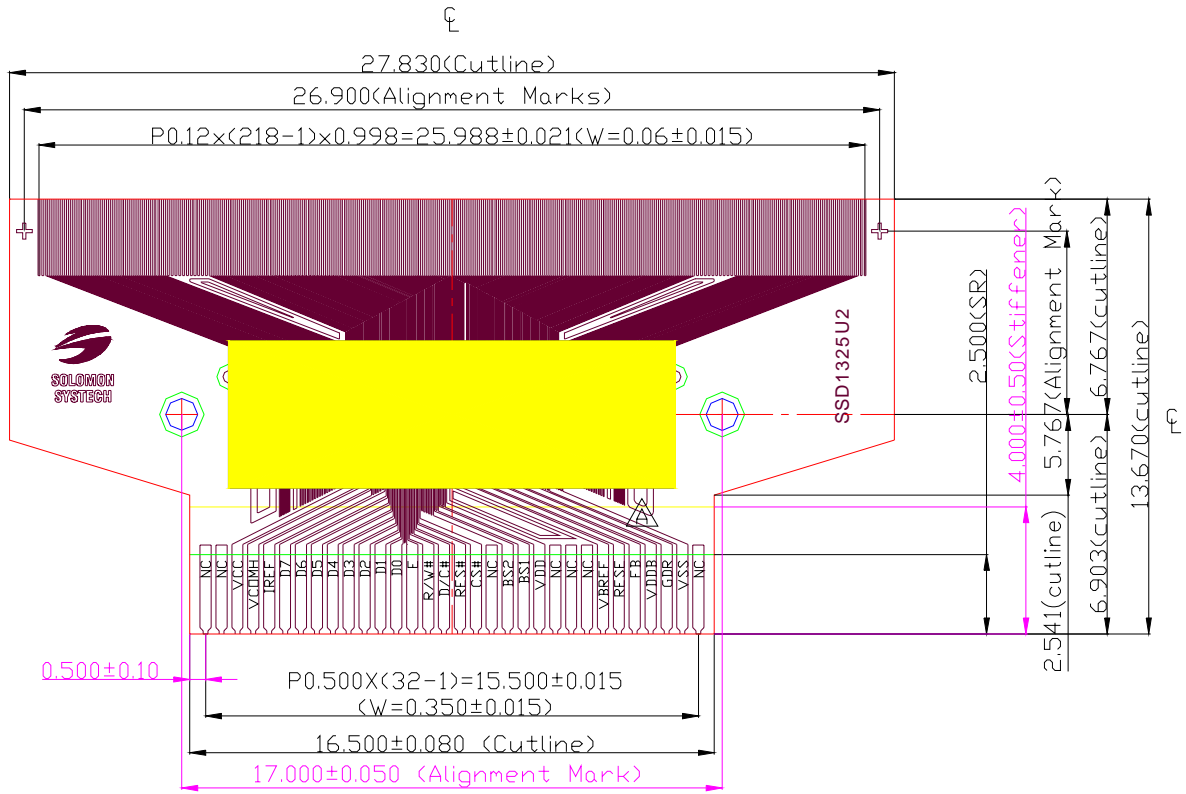
Pin #	Pin Name	X-Axis	Y-Axis
61	COM9	9.54	12.125
62	COM7	9.42	12.325
63	COM5	9.3	12.125
64	COM3	9.18	12.325
65	COM1	9.06	12.125
66	NC	8.94	12.325
67	NC	8.82	12.125
68	NC	8.7	12.325
69	NC	8.58	12.125
70	NC	8.46	12.325
71	NC	8.34	12.125
72	NC	8.22	12.325
73	NC	8.1	12.125
74	NC	7.98	12.325
75	NC	7.86	12.125
76	NC	7.74	12.325
77	SEG127	7.62	12.125
78	SEG126	7.5	12.325
79	SEG125	7.38	12.125
80	SEG124	7.26	12.325
81	SEG123	7.14	12.125
82	SEG122	7.02	12.325
83	SEG121	6.9	12.125
84	SEG120	6.78	12.325
85	SEG119	6.66	12.125
86	SEG118	6.54	12.325
87	SEG117	6.42	12.125
88	SEG116	6.3	12.325
89	SEG115	6.18	12.125
90	SEG114	6.06	12.325
91	SEG113	5.94	12.125
92	SEG112	5.82	12.325
93	SEG111	5.7	12.125
94	SEG110	5.58	12.325
95	SEG109	5.46	12.125
96	SEG108	5.34	12.325
97	SEG107	5.22	12.125
98	SEG106	5.1	12.325
99	SEG105	4.98	12.125
100	SEG104	4.86	12.325
101	SEG103	4.74	12.125
102	SEG102	4.62	12.325
103	SEG101	4.5	12.125
104	SEG100	4.38	12.325
105	SEG99	4.26	12.125
106	SEG98	4.14	12.325
107	SEG97	4.02	12.125
108	SEG96	3.9	12.325
109	SEG95	3.78	12.125
110	SEG94	3.66	12.325
111	SEG93	3.54	12.125
112	SEG92	3.42	12.325
113	SEG91	3.3	12.125
114	SEG90	3.18	12.325
115	SEG89	3.06	12.125
116	SEG88	2.94	12.325
117	SEG87	2.82	12.125
118	SEG86	2.7	12.325
119	SEG85	2.58	12.125
120	SEG84	2.46	12.325

Pin #	Pin Name	X-Axis	Y-Axis
121	SEG83	2.34	12.125
122	SEG82	2.22	12.325
123	SEG81	2.1	12.125
124	SEG80	1.98	12.325
125	SEG79	1.86	12.125
126	SEG78	1.74	12.325
127	SEG77	1.62	12.125
128	SEG76	1.5	12.325
129	SEG75	1.38	12.125
130	SEG74	1.26	12.325
131	SEG73	1.14	12.125
132	SEG72	1.02	12.325
133	SEG71	0.9	12.125
134	SEG70	0.78	12.325
135	SEG69	0.66	12.125
136	SEG68	0.54	12.325
137	SEG67	0.42	12.125
138	SEG66	0.3	12.325
139	SEG65	0.18	12.125
140	SEG64	0.06	12.325
141	SEG63	-0.06	12.125
142	SEG62	-0.18	12.325
143	SEG61	-0.3	12.125
144	SEG60	-0.42	12.325
145	SEG59	-0.54	12.125
146	SEG58	-0.66	12.325
147	SEG57	-0.78	12.125
148	SEG56	-0.9	12.325
149	SEG55	-1.02	12.125
150	SEG54	-1.14	12.325
151	SEG53	-1.26	12.125
152	SEG52	-1.38	12.325
153	SEG51	-1.5	12.125
154	SEG50	-1.62	12.325
155	SEG49	-1.74	12.125
156	SEG48	-1.86	12.325
157	SEG47	-1.98	12.125
158	SEG46	-2.1	12.325
159	SEG45	-2.22	12.125
160	SEG44	-2.34	12.325
161	SEG43	-2.46	12.125
162	SEG42	-2.58	12.325
163	SEG41	-2.7	12.125
164	SEG40	-2.82	12.325
165	SEG39	-2.94	12.125
166	SEG38	-3.06	12.325
167	SEG37	-3.18	12.125
168	SEG36	-3.3	12.325
169	SEG35	-3.42	12.125
170	SEG34	-3.54	12.325
171	SEG33	-3.66	12.125
172	SEG32	-3.78	12.325
173	SEG31	-3.9	12.125
174	SEG30	-4.02	12.325
175	SEG29	-4.14	12.125
176	SEG28	-4.26	12.325
177	SEG27	-4.38	12.125
178	SEG26	-4.5	12.325
179	SEG25	-4.62	12.125
180	SEG24	-4.74	12.325

Pin #	Pin Name	X-Axis	Y-Axis
181	SEG23	-4.86	12.125
182	SEG22	-4.98	12.325
183	SEG21	-5.1	12.125
184	SEG20	-5.22	12.325
185	SEG19	-5.34	12.125
186	SEG18	-5.46	12.325
187	SEG17	-5.58	12.125
188	SEG16	-5.7	12.325
189	SEG15	-5.82	12.125
190	SEG14	-5.94	12.325
191	SEG13	-6.06	12.125
192	SEG12	-6.18	12.325
193	SEG11	-6.3	12.125
194	SEG10	-6.42	12.325
195	SEG9	-6.54	12.125
196	SEG8	-6.66	12.325
197	SEG7	-6.78	12.125
198	SEG6	-6.9	12.325
199	SEG5	-7.02	12.125
200	SEG4	-7.14	12.325
201	SEG3	-7.26	12.125
202	SEG2	-7.38	12.325
203	SEG1	-7.5	12.125
204	SEG0	-7.62	12.325
205	NC	-7.74	12.125
206	NC	-7.86	12.325
207	NC	-7.98	12.125
208	NC	-8.1	12.325
209	NC	-8.22	12.125
210	NC	-8.34	12.325
211	NC	-8.46	12.125
212	NC	-8.58	12.325
213	NC	-8.7	12.125
214	NC	-8.82	12.325
215	NC	-8.94	12.125
216	COM0	-9.06	12.325
217	COM2	-9.18	12.125
218	COM4	-9.3	12.325
219	COM6	-9.42	12.125
220	COM8	-9.54	12.325
221	COM10	-9.66	12.125
222	COM12	-9.78	12.325
223	COM14	-9.9	12.125
224	COM16	-10.02	12.325
225	COM18	-10.14	12.125
226	COM20	-10.26	12.325
227	COM22	-10.38	12.125
228	COM24	-10.5	12.325
229	COM26	-10.62	12.125
230	COM28	-10.74	12.325
231	COM30	-10.86	12.125
232	COM32	-10.98	12.325
233	COM34	-11.1	12.125
234	COM36	-11.22	12.325
235	COM38	-11.34	12.125
236	COM40	-11.46	12.325
237	COM42	-11.58	12.125
238	COM44	-11.7	12.325
239	COM46	-11.82	12.125
240	COM48	-11.94	12.325

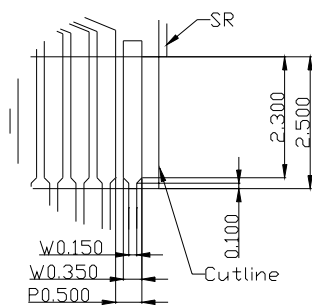
Pin #	Pin Name	X-Axis	Y-Axis
241	COM50	-12.06	12.125
242	COM52	-12.18	12.325
243	COM54	-12.3	12.125
244	COM56	-12.42	12.325
245	COM58	-12.54	12.125
246	COM60	-12.66	12.325
247	COM62	-12.78	12.125
248	NC	-12.9	12.325
249	NC	-13.02	12.125

# SSD1325U2 COF Package Dimensions

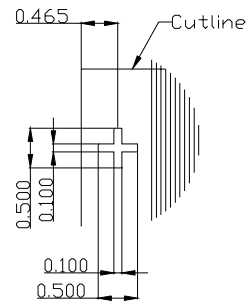


## NOTE:

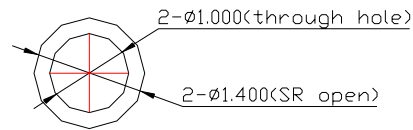
1. GENERAL TOLERANCE:  $\pm 0.05$ mm
2. CUTLINE TOLERANCE:  $\pm 0.15$ mm
3. MATERIAL
  - PI:  $38 \pm 4$ um
  - CU:  $8 \pm 2$ um
  - SR:  $15 \pm 10$ um
4. SN PLATING:  $0.20 \pm 0.05$ um
5. SOLOMON SYSTECH INTERNAL USE ONLY WHICH MAY BE REPLACED BY PUNCHING HOLE
6. Min Pitch 43um ; Min Space 23um



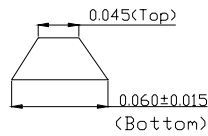
Detail A (2:1)



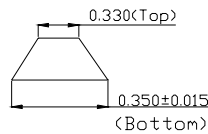
Detail B (3:1)



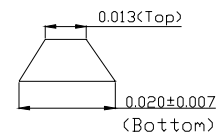
Alignment Mark (3:1)



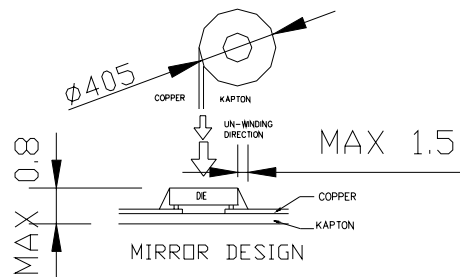
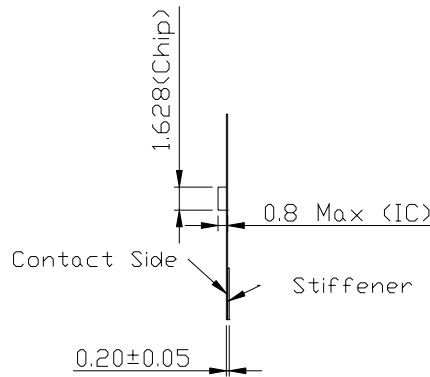
Output Side Lead cross section



Input Side Lead cross section



Output Side Inner Lead cross section



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