SSD1328

Advance Information

128 x 128, 16 Gray Scale Dot Matrix OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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GENERAL DESCRIPTION

SSD1328 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SSD1328 consists of 256 high voltage/current driving output pins for driving 128 segments and 128 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1328 displays data directly from its internal 128x128x4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

SSD1328 has a 128-step contrast control and a 16 gray level control. The embedded on-chip oscillator reduces the number of external components.

FEATURES

- Support max. 128 x 128 matrix panel
- Power supply: VDD=2.4V - 3.5V, VCC=8.0V - 18.0V
- OLED driving output voltage, 16V maximum
- Segment maximum source current: 300uA
- Common maximum sink current: 40mA
- Embedded 128 x 128 x 4 bit SRAM display buffer
- External current reference
- 128 step contrast control on monochrome passive OLED panel
- 16 gray scale
- On-Chip Oscillator
- Programmable Frame Rate/Pre-charge voltage
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Row re-mapping and Column re-mapping
- Vertical scrolling
- Support Partial display
- Low power consumption (<5.0uA @sleep mode)
- Wide range of operating temperature: -30 to 90 °C

ORDERING INFORMATION

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1328Z	128	128	COG	Page 8	Die Size: 11.41mm x 1.63mm Die Thickness: 457 +/- 25um I/O pad pitch (a): 76.2um SEG pad pitch (b): 52.2um COM pad pitch (c): 51.8um
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BLOCK DIAGRAM

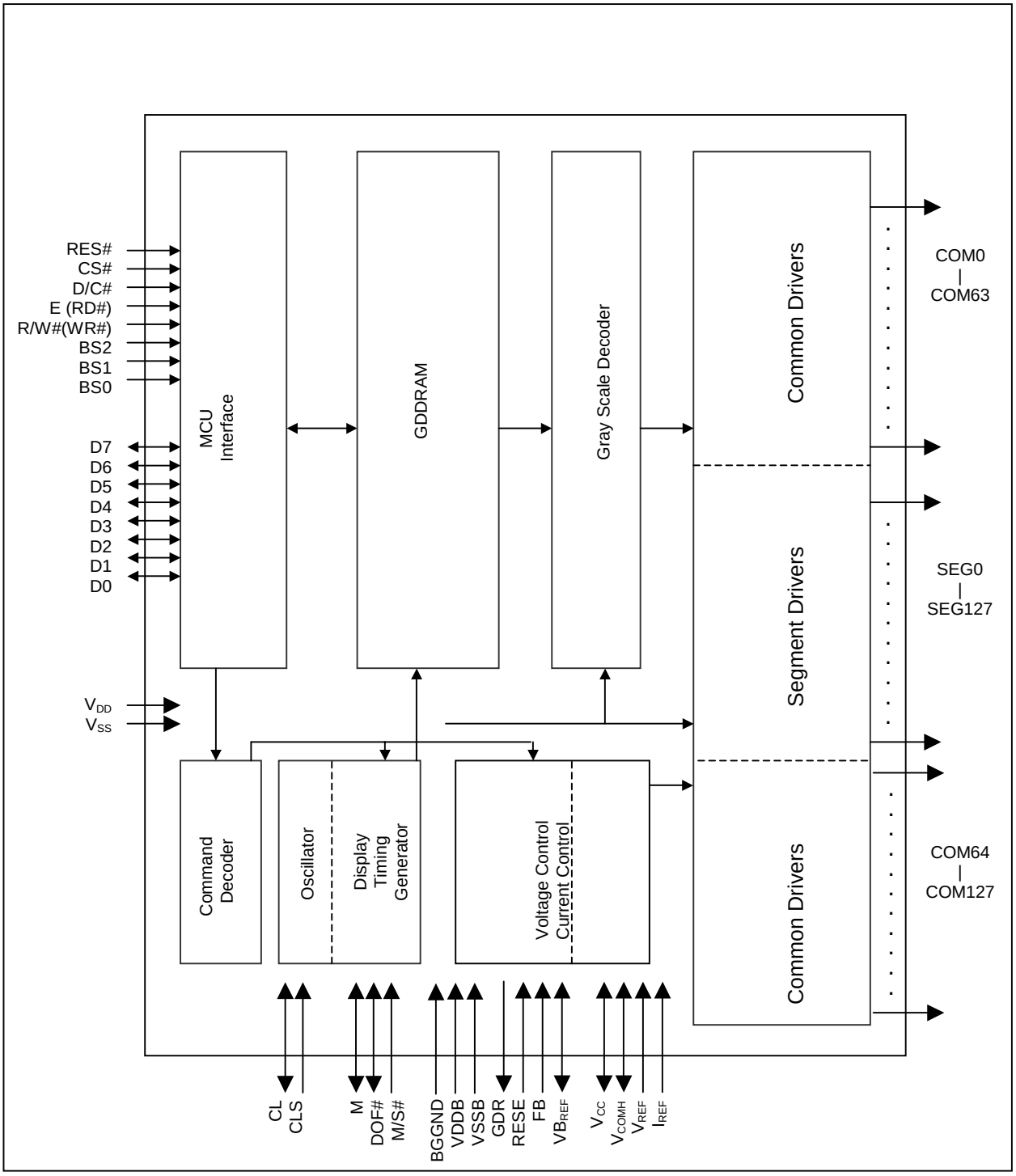
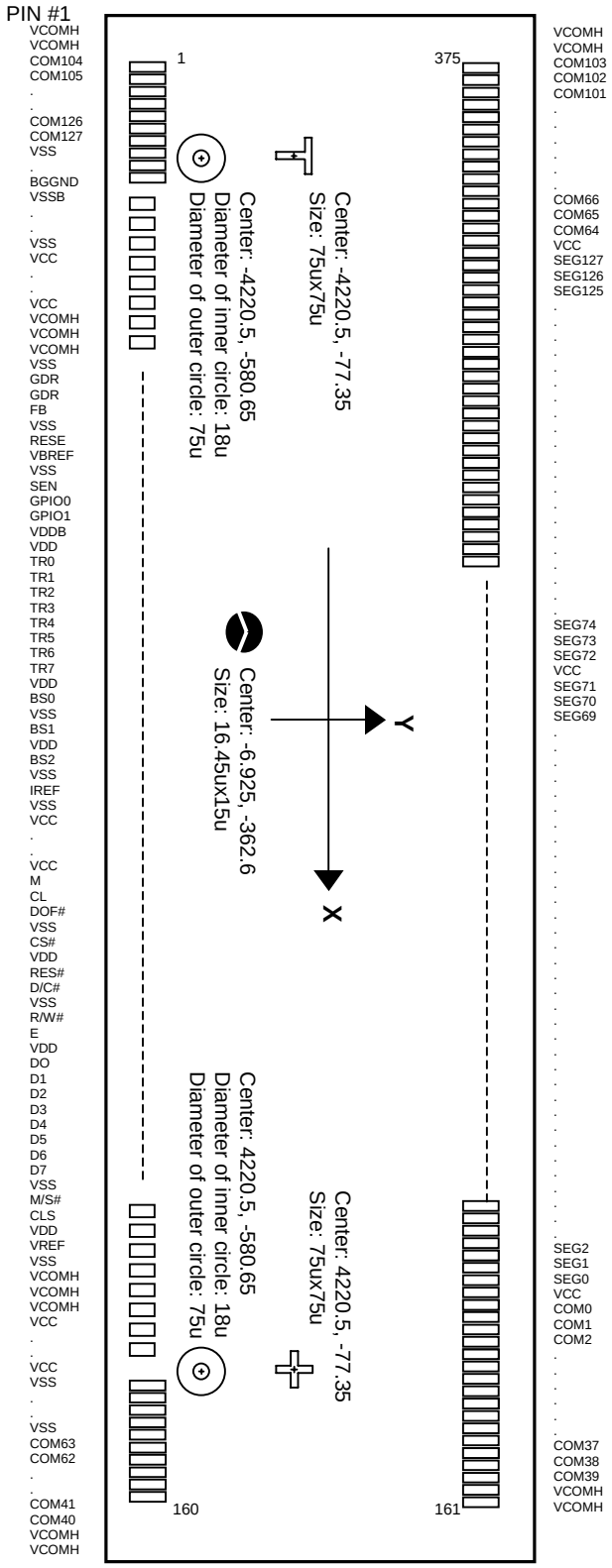


Figure 1 - Block Diagram

SSD1328Z GOLD BUMP DIE PAD ASSIGNMENT



+ represents the centre of the alignment mark

TR0-TR7, GPIO0, GPIO1
These are reserved pins. No connection should be made for these pins and left float individually.

Die Size: 11.41mm x 1.63mm
Die Thickness: 457 +/- 25um
I/O pad pitch (a): 76.2um
SEG pad pitch (b): 52.2um
COM pad pitch (c): 51.8um
Bump Height: Nominal 18um

Figure 2 - SSD1328Z Gold bump die pad assignment

SSD1328Z Die Pad Coordinates

Pad#	Signal	X-pos	Y-pos
1	VCOMH	-5619.9	-636.8
2	VCOMH	-5568.1	-636.8
3	COM104	-5516.3	-636.8
4	COM105	-5464.5	-636.8
5	COM106	-5412.7	-636.8
6	COM107	-5360.9	-636.8
7	COM108	-5309.1	-636.8
8	COM109	-5257.3	-636.8
9	COM110	-5205.5	-636.8
10	COM111	-5153.7	-636.8
11	COM112	-5101.9	-636.8
12	COM113	-5050.1	-636.8
13	COM114	-4998.3	-636.8
14	COM115	-4946.5	-636.8
15	COM116	-4894.7	-636.8
16	COM117	-4842.9	-636.8
17	COM118	-4791.1	-636.8
18	COM119	-4739.3	-636.8
19	COM120	-4687.5	-636.8
20	COM121	-4635.7	-636.8
21	COM122	-4583.9	-636.8
22	COM123	-4532.1	-636.8
23	COM124	-4480.3	-636.8
24	COM125	-4428.5	-636.8
25	COM126	-4376.7	-636.8
26	COM127	-4324.9	-636.8
27	VSS	-4239.8	-674.65
28	VSS	-4163.6	-674.65
29	VSS	-4087.4	-674.65
30	VSS	-4011.2	-674.65
31	BGGND	-3935	-674.65
32	VSSB	-3858.8	-674.65
33	VSSB	-3782.6	-674.65
34	VSS	-3706.4	-674.65
35	VSS	-3630.2	-674.65
36	VSS	-3554	-674.65
37	VSS	-3477.8	-674.65
38	VSS	-3401.6	-674.65
39	VSS	-3325.4	-674.65
40	VSS	-3249.2	-674.65
41	VSS	-3159.3	-644.25
42	VCC	-3083.1	-644.25
43	VCC	-3006.9	-644.25
44	VCC	-2930.7	-644.25
45	VCC	-2854.5	-644.25
46	VCOMH	-2778.3	-644.25
47	VCOMH	-2702.1	-644.25
48	VCOMH	-2625.9	-644.25
49	VSS	-2549.7	-644.25
50	GDR	-2451.4	-644.25
51	GDR	-2375.2	-644.25
52	FB	-2048.7	-644.25
53	VSS	-1968.1	-644.25
54	RESE	-1891.9	-644.25
55	VBREF	-1815.7	-644.25
56	VSS	-1739.5	-644.25
57	SEN	-1663.3	-644.25
58	GPIO0	-1592.7	-644.25
59	GPIO1	-1502.1	-644.25
60	VDDB	-1425.9	-644.25
61	VDD	-1349.7	-644.25
62	TR0	-1273.5	-644.25
63	TR1	-1197.3	-644.25
64	TR2	-1121.1	-644.25
65	TR3	-1044.9	-644.25
66	TR4	-968.7	-644.25
67	TR5	-892.5	-644.25
68	TR6	-816.3	-644.25
69	TR7	-740.1	-644.25
70	VDD	-663.9	-644.25
71	BS0	-587.7	-644.25
72	VSS	-511.5	-644.25
73	BS1	-435.3	-644.25
74	VDD	-359.1	-644.25
75	BS2	-282.9	-644.25
76	VSS	-202.3	-644.25
77	IREF	-126.1	-644.25
78	VSS	-49.9	-644.25
79	VCC	26.3	-644.25
80	VCC	102.5	-644.25
81	VCC	178.7	-644.25
82	VCC	254.9	-644.25
83	VCC	331.1	-644.25
84	VCC	407.3	-644.25
85	M	487.9	-644.25
86	CL	564.1	-644.25
87	DOF#	640.3	-644.25
88	VSS	716.5	-644.25
89	CS#	792.7	-644.25
90	VDD	868.9	-644.25
91	RES#	945.1	-644.25
92	D/C#	1021.3	-644.25
93	VSS	1097.5	-644.25
94	R/W#	1173.7	-644.25
95	E	1249.9	-644.25
96	VDD	1326.1	-644.25
97	D0	1402.3	-644.25
98	D1	1478.5	-644.25
99	D2	1554.7	-644.25
100	D2	1630.9	-644.25
101	D3	1707.1	-644.25
102	D4	1783.3	-644.25
103	D5	1859.5	-644.25
104	D6	1935.7	-644.25
105	D7	2011.9	-644.25
106	VSS	2088.1	-644.25
107	M/S#	2164.3	-644.25
108	CLS	2240.5	-644.25
109	VDD	2316.7	-644.25
110	VREF	2397.3	-644.25
111	VSS	2473.5	-644.25
112	VCOMH	2549.7	-644.25
113	VCOMH	2625.9	-644.25
114	VCOMH	2702.1	-644.25
115	VCC	2778.3	-644.25
116	VCC	2854.5	-644.25
117	VCC	2930.7	-644.25
118	VCC	3006.9	-644.25
119	VSS	3083.1	-644.25
120	VSS	3173	-686.15
121	VSS	3249.2	-686.15
122	VSS	3325.4	-686.15
123	VSS	3401.6	-686.15
124	VSS	3477.8	-686.15
125	VSS	3554	-686.15
126	VSS	3630.2	-686.15
127	VSS	3706.4	-686.15
128	VSS	3782.6	-686.15
129	VSS	3858.8	-686.15
130	VSS	3935	-686.15
131	VSS	4011.2	-686.15
132	VSS	4087.4	-686.15
133	VSS	4163.6	-686.15
134	VSS	4239.8	-686.15
135	COM63	4324.9	-636.8
136	COM62	4376.7	-636.8
137	COM61	4428.5	-636.8
138	COM60	4480.3	-636.8
139	COM59	4532.1	-636.8
140	COM58	4583.9	-636.8
141	COM57	4635.7	-636.8
142	COM56	4687.5	-636.8
143	COM55	4739.3	-636.8
144	COM54	4791.1	-636.8
145	COM53	4842.9	-636.8
146	COM52	4894.7	-636.8
147	COM51	4946.5	-636.8
148	COM50	4998.3	-636.8
149	COM49	5050.1	-636.8
150	COM48	5101.9	-636.8
151	COM47	5153.7	-636.8
152	COM46	5205.5	-636.8
153	COM45	5257.3	-636.8
154	COM44	5309.1	-636.8
155	COM43	5360.9	-636.8
156	COM42	5412.7	-636.8
157	COM41	5464.5	-636.8
158	COM40	5516.3	-636.8
159	VCOMH	5568.1	-636.8
160	VCOMH	5619.9	-636.8
161	VCOMH	5619.9	624.8
162	VCOMH	5568.1	624.8
163	COM39	5516.3	624.8
164	COM38	5464.5	624.8
165	COM37	5412.7	624.8
166	COM36	5360.9	624.8
167	COM35	5309.1	624.8
168	COM34	5257.3	624.8
169	COM33	5205.5	624.8
170	COM32	5153.7	624.8
171	COM31	5101.9	624.8
172	COM30	5050.1	624.8
173	COM29	4998.3	624.8
174	COM28	4946.5	624.8
175	COM27	4894.7	624.8
176	COM26	4842.9	624.8
177	COM25	4791.1	624.8
178	COM24	4739.3	624.8
179	COM23	4687.5	624.8
180	COM22	4635.7	624.8
181	COM21	4583.9	624.8
182	COM20	4532.1	624.8
183	COM19	4480.3	624.8
184	COM18	4428.5	624.8
185	COM17	4376.7	624.8
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187	COM15	4273.1	624.8
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189	COM13	4169.5	624.8
190	COM12	4117.7	624.8
191	COM11	4065.9	624.8
192	COM10	4014.1	624.8
193	COM9	3962.3	624.8
194	COM8	3910.5	624.8
195	COM7	3858.7	624.8
196	COM6	3806.9	624.8
197	COM5	3755.1	624.8
198	COM4	3703.3	624.8
199	COM3	3651.5	624.8
200	COM2	3599.7	624.8
201	COM1	3547.9	624.8
202	COM0	3496.1	624.8
203	VCC	3392.9	624.8
204	SEG0	3340.7	624.8
205	SEG1	3288.5	624.8
206	SEG2	3236.3	624.8
207	SEG3	3184.1	624.8
208	SEG4	3131.9	624.8
209	SEG5	3079.7	624.8
210	SEG6	3027.5	624.8
211	SEG7	2975.3	624.8
212	SEG8	2923.1	624.8
213	SEG9	2870.9	624.8
214	SEG10	2818.7	624.8
215	SEG11	2766.5	624.8
216	SEG12	2714.3	624.8
217	SEG13	2662.1	624.8
218	SEG14	2609.9	624.8
219	SEG15	2557.7	624.8
220	SEG16	2505.5	624.8
221	SEG17	2453.3	624.8
222	SEG18	2401.1	624.8
223	SEG19	2348.9	624.8
224	SEG20	2296.7	624.8
225	SEG21	2244.5	624.8
226	SEG22	2192.3	624.8
227	SEG23	2140.1	624.8
228	SEG24	2087.9	624.8
229	SEG25	2035.7	624.8
230	SEG26	1983.5	624.8
231	SEG27	1931.3	624.8
232	SEG28	1879.1	624.8
233	SEG29	1826.9	624.8
234	SEG30	1774.7	624.8
235	SEG31	1722.5	624.8
236	SEG32	1670.3	624.8
237	SEG33	1618.1	624.8
238	SEG34	1565.9	624.8
239	SEG35	1513.7	624.8
240	SEG36	1461.5	624.8
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242	SEG38	1357.1	624.8
243	SEG39	1304.9	624.8
244	SEG40	1252.7	624.8
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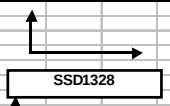
252	SEG48	835.1	624.8
253	SEG49	782.9	624.8
254	SEG50	730.7	624.8
255	SEG51	678.5	624.8
256	SEG52	626.3	624.8
257	SEG53	574.1	624.8
258	SEG54	521.9	624.8
259	SEG55	469.7	624.8
260	SEG56	417.5	624.8
261	SEG57	365.3	624.8
262	SEG58	313.1	624.8
263	SEG59	260.9	624.8
264	SEG60	208.7	624.8
265	SEG61	156.5	624.8
266	SEG62	104.3	624.8
267	SEG63	52.1	624.8
268	SEG64	-0.1	624.8
269	SEG65	-52.3	624.8
270	SEG66	-104.5	624.8
271	SEG67	-156.7	624.8
272	SEG68	-208.9	624.8
273	SEG69	-261.1	624.8
274	SEG70	-313.3	624.8
275	SEG71	-365.5	624.8
276	VCC	-417.7	624.8
277	SEG72	-469.9	624.8
278	SEG73	-522.1	624.8
279	SEG74	-574.3	624.8
280	SEG75	-626.5	624.8
281	SEG76	-678.7	624.8
282	SEG77	-730.9	624.8
283	SEG78	-783.1	624.8
284	SEG79	-835.3	624.8
285	SEG80	-887.5	624.8
286	SEG81	-939.7	624.8
287	SEG82	-991.9	624.8
288	SEG83	-1044.1	624.8
289	SEG84	-1096.3	624.8
290	SEG85	-1148.5	624.8
291	SEG86	-1200.7	624.8
292	SEG87	-1252.9	624.8
293	SEG88	-1305.1	624.8
294	SEG89	-1357.3	624.8
295	SEG90	-1409.5	624.8
296	SEG91	-1461.7	624.8
297	SEG92	-1513.9	624.8
298	SEG93	-1566.1	624.8
299	SEG94	-1618.3	624.8
300	SEG95	-1670.5	624.8
301	SEG96	-1722.7	624.8
302	SEG97	-1774.9	624.8
303	SEG98	-1827.1	624.8
304	SEG99	-1879.3	624.8
305	SEG100	-1931.5	624.8
306	SEG101	-1983.7	624.8
307	SEG102	-2035.9	624.8
308	SEG103	-2088.1	624.8
309	SEG104	-2140.3	624.8
310	SEG105	-2192.5	624.8
311	SEG106	-2244.7	624.8
312	SEG107	-2296.9	624.8
313	SEG108	-2349.1	624.8
314	SEG109	-2401.3	624.8
315	SEG110	-2453.5	624.8
316	SEG111	-2505.7	624.8
317	SEG112	-2557.9	624.8
318	SEG113	-2610.1	624.8
319	SEG114	-2662.3	624.8
320	SEG115	-2714.5	624.8
321	SEG116	-2766.7	624.8
322	SEG117	-2818.9	624.8
323	SEG118	-2871.1	624.8
324	SEG119	-2923.3	624.8
325	SEG120	-2975.5	624.8
326	SEG121	-3027.7	624.8
327	SEG122	-3079.9	624.8
328	SEG123	-3132.1	624.8
329	SEG124	-3184.3	624.8
330	SEG125	-3236.5	624.8
331	SEG126	-3288.7	624.8
332	SEG127	-3340.9	624.8
333	VCC	-3393.1	624.8
334	COM64	-3496.1	624.8
335	COM65	-3547.9	624.8
336	COM66	-3599.7	624.8
337	COM67	-3651.5	624.8
338	COM68	-3703.3	624.8
339	COM69	-3755.1	624.8
340	COM70	-3806.9	624.8
341	COM71	-3858.7	624.8
342	COM72	-3910.5	624.8
343	COM73	-3962.3	624.8
344	COM74	-4014.1	624.8
345	COM75	-4065.9	624.8
346	COM76	-4117.7	624.8
347	COM77	-4169.5	624.8
348	COM78	-4221.3	624.8
349	COM79	-4273.1	624.8
350	COM80	-4324.9	624.8
351	COM81	-4376.7	624.8
352	COM82	-4428.5	624.8
353	COM83	-4480.3	624.8
354	COM84	-4532.1	624.8
355	COM85	-4583.9	624.8
356	COM86	-4635.7	624.8
357	COM87	-4687.5	624.8
358	COM88	-4739.3	624.8
359	COM89	-4791.1	624.8
360	COM90	-4842.9	624.8
361	COM91	-4894.7	624.8
362	COM92	-4946.5	624.8
363	COM93	-4998.3	624.8
364	COM94	-5050.1	624.8
365	COM95	-5101.9	624.8
366	COM96	-5153.7	624.8
367	COM97	-5205.5	624.8
368	COM98	-5257.3	624.8
369	COM99	-5309.1	624.8
370	COM100	-5360.9	624.8
371	COM101	-5412.7	624.8
372	COM102	-5464.5	624.8
373	COM103	-5516.3	624.8
374	VCOMH	-5568.1	624.8
375	VCOMH	-5619.9	624.8



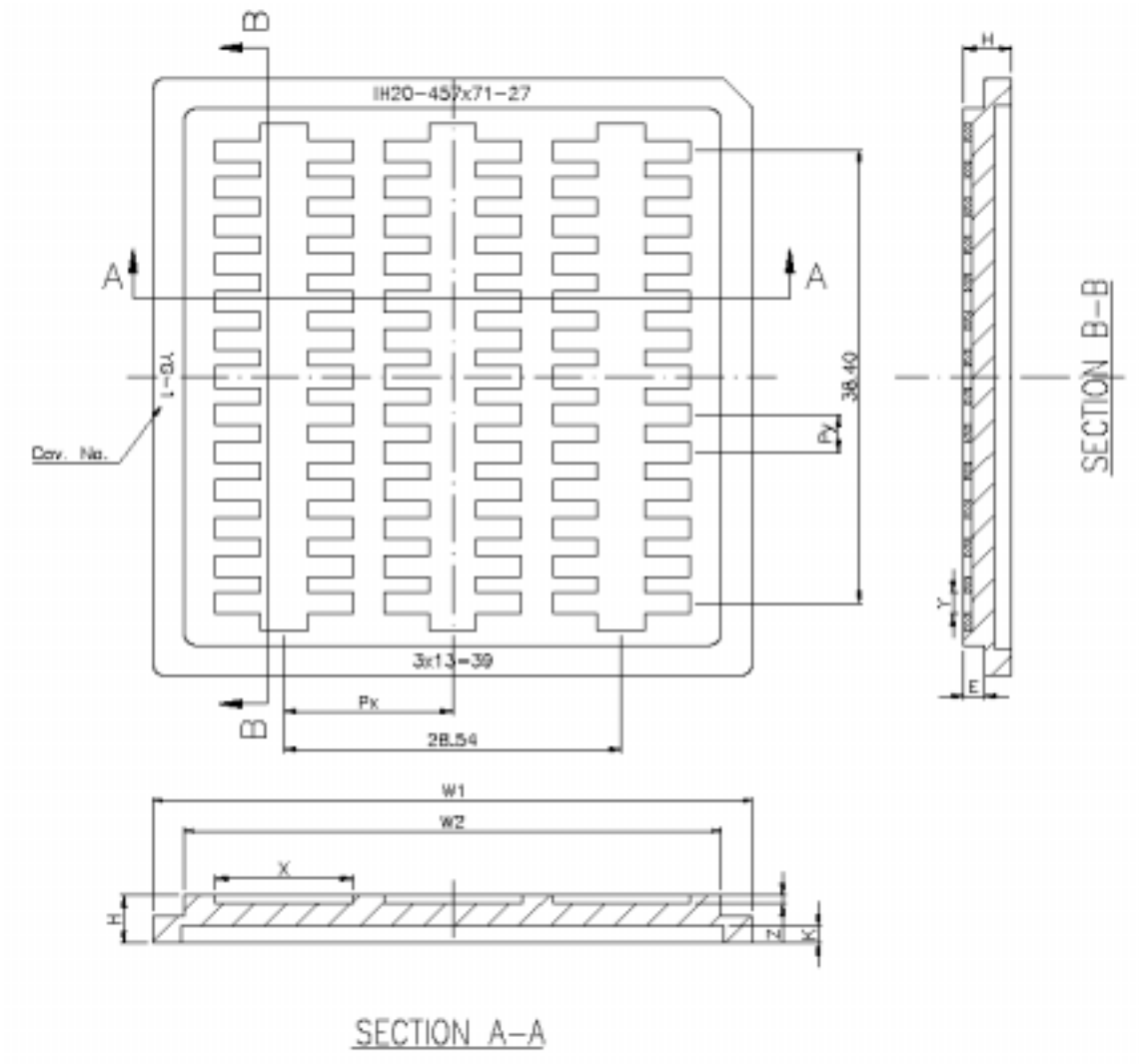
Pad 1,2,3,? >160
Gold Bumps face up

Bump size:

Pad 1-26,135-375:
34um x 84um
Pad 27-40:
56um x 56um
Pad 41-134:
56um x 79um

Table 1 - SSD1328Z Gold bump die pad coordinates

SSD1328Z DIE TRAY DIMENSIONS



Parameter	Dimensions
W1	50.70±0.2mm
W2	45.50±0.2mm
H	4.05±0.2mm
E	1.75±0.2mm
K	1.45±0.2mm
Px	14.27±0.1mm
Py	3.20±0.1mm
X	11.60±0.1mm
Y	1.80±0.1mm
Z	0.68±0.05mm
N (number of die)	39

PIN DESCRIPTION

M, DOF#
These pins are No Connection pins. Nothing should be connected to these pins, nor they are connected together. These pins should be left open individually.

CL
This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. In this case, the output clock frequency equals to the internal clock frequency. When internal oscillator is disabled, this pin receives display clock signal from external clock source.

M/S#
This pin is an input pin and must be pulled high to enable the chip function.

CLS
This pin is internal clock enable. When this pin is pulled high, internal clock is enabled.
The internal clock will be disabled when it is pulled low, an external clock source must be connected to CL pin for normal operation.

BS0, BS1, BS2
These pins are MCU interface selection input. See the following table:

	6800-parallel interface	8080-parallel interface	Serial interface
BS0	0	0	0
BS1	0	1	0
BS2	1	1	0

Table 2 - MCU interface setting

CS#
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

RES#
This pin is reset signal input. When the pin is low, initialization of the chip is executed.

D/C#
This pin is Data/Command control pin. When the pin is pulled high, the input at D_7-D_0 is treated as display data. When the pin is pulled low, the input at D_7-D_0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/W#(WR#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “LOW” for write mode.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.

E (RD#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.

D_7-D_0
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D_1 will be the serial data input SDIN and D_0 will be the serial clock input SCLK.

V_{DD}
This is a voltage supply pin. It must be connected to external source.

V_{SS}
This is a ground pin. It also acts as a reference for the logic pins and the OLED driving voltages. It must be connected to external ground.

V_{CC}
This is the most positive voltage supply pin of the chip. It is supplied externally.

V_{REF}
This pin is the voltage reference for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can be either supplied externally or connected to V_{CC}.

I_{REF}
This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 10uA. See setting in application example on page 32.

V_{COMH}
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.

VDDB
This is power pin. It should be connected to V_{DD}.

VSSB
This is ground pin. It must be connected to external ground.

GDR
This is used for testing purpose. It should be left open under normal operation.

RESE
This is used for testing purpose. It should be left open under normal operation.

VB_{REF}
This is used for testing purpose. It should be left open under normal operation.

FB
This is used for testing purpose. It should be left open under normal operation.

BGGND
This is a ground pin for analog circuits. It must be connected to external ground.

COM0-COM127
These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off.

SEG0-SEG127
These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off.

FUNCTIONAL BLOCK DESCRIPTIONS

Command Decoder
This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.
If D/C# pin is high, the input at D_7-D_0 is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D_7-D_0 is interpreted as a Command which will be decoded and be written to the corresponding command register.

MPU Parallel 6800-series Interface
The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/W#(WR#), D/C#, E (RD#), CS#. R/W#(WR#) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W# (WR#) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C# input. The E (RD#) input serves as data latch signal (clock) when high provided that CS# is low. Refer to Parallel Interface Timing Diagram of 6800-series microprocessors.
In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3 below.

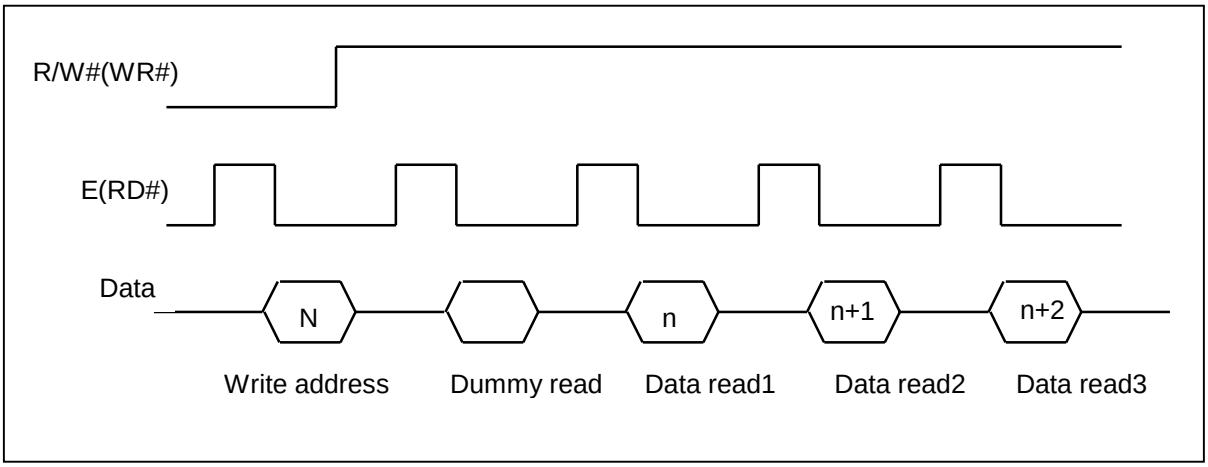


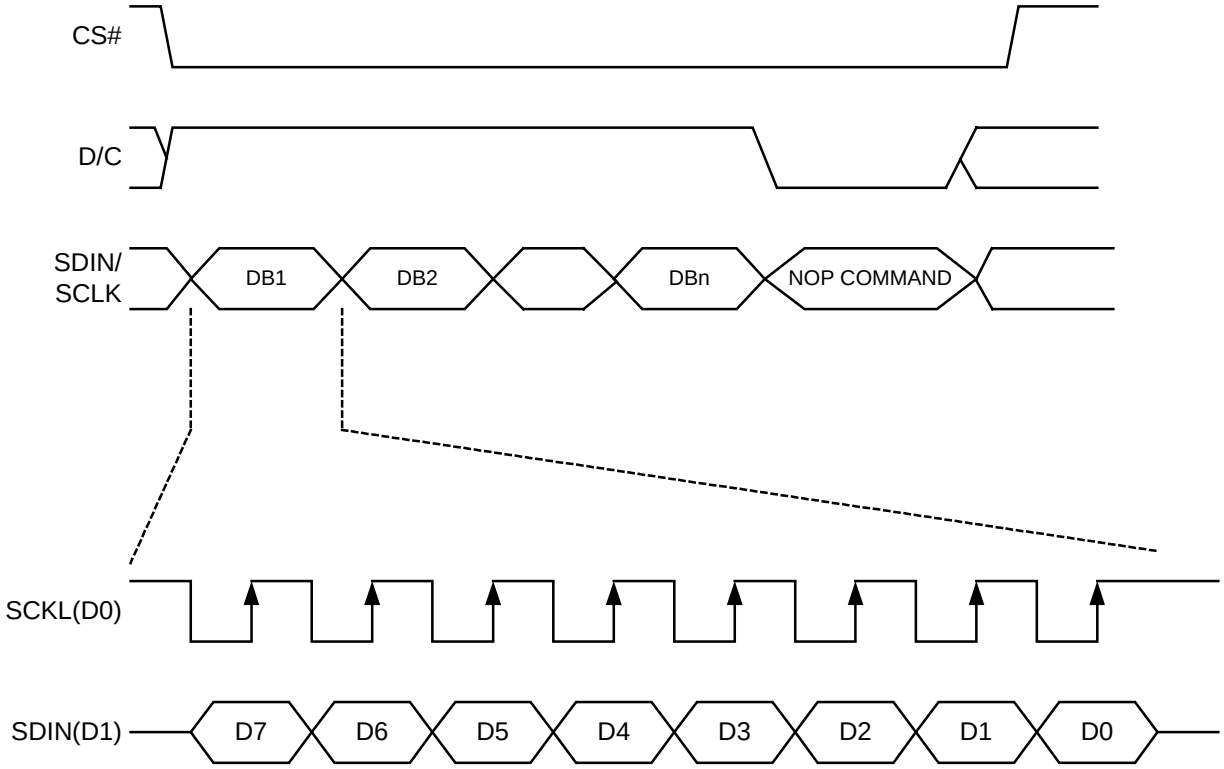
Figure 3 - Display Data Read Back Procedure - Insertion of Dummy Read

MPU Parallel 8080-series Interface
The parallel interface consists of 8 bi-directional data pins (D_7-D_0), E (RD#), R/W#(WR#), D/C#, CS#. The E (RD#) input serves as data read latch signal (clock) when it is low, and provided that CS# is low. Display data or status register read is controlled by D/C#.
R/W# (WR#) input serves as data write latch signal (clock) when it is high and provided that CS# is low. Display data or command register write is controlled by D/C#. Refer to Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial Interface
The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D_7, D_6, ... D_0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

During data writing, an additional NOP command should be inserted before the CS# goes high (Refer to Figure 4.

Figure 4 - Display data write procedure in SPI mode



Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128x128 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 40H
9. Set quarter current range

Oscillator Circuit and Display Time Generator

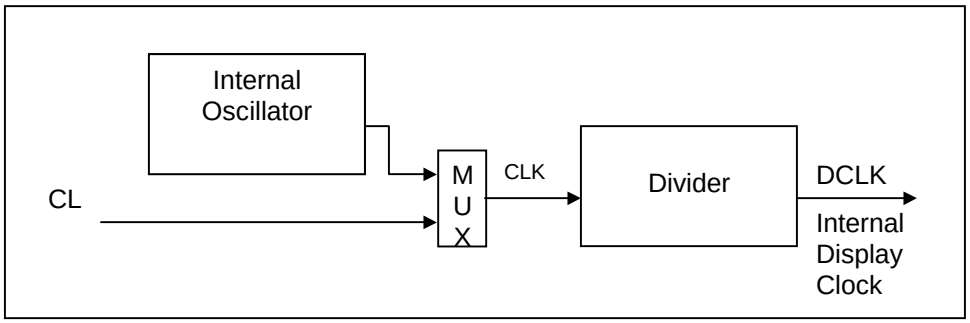


Figure 5 - Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 5). The oscillator generates the clock for the Display Timing Generator.

Current Control and Voltage Control

This block is used to derive the incoming power sources into the different levels of internal use voltage and current. V_{CC} and V_{DD} are external power supplies. V_{REF} is reference voltage, which is used to derive driving voltage for segments and commons. I_{REF} is a reference current source for segment current drivers.

Segment Drivers/Common Drivers

Segment drivers deliver 128 current sources to drive OLED panel. The driving current can be adjusted from 0 to 300uA with 128 steps. Common drivers generate voltage scanning pulse.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. See the description of the GDDRAM address map in Table 3 -Table 7 on page16 - 18.
For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.
For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display. Table 6 shows the example in which the display start line register is set to 78H.

Graphic Display Data RAM (GDDRAM) Address Map

Table 3 - GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 … D8191)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs
Column Address (HEX)

COM Outputs
Row Address (HEX)

Nibble Re-map A[1]=0

Table 4 - GDDRAM Address Map - Vertical Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 … D8191)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D128[3:0]	D128[7:4]		D7936[3:0]	D7936[7:4]	D8064[3:0]	D8064[7:4]
COM1	01	D1[3:0]	D1[7:4]	D129[3:0]	D129[7:4]		D7937[3:0]	D7937[7:4]	D8065[3:0]	D8065[7:4]
|	|									
COM126	7E	D126[3:0]	D126[7:4]	D254[3:0]	D254[7:4]		D8062[3:0]	D8062[7:4]	D8190[3:0]	D8190[7:4]
COM127	7F	D127[3:0]	D127[7:4]	D255[3:0]	D255[7:4]		D8063[3:0]	D8063[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs

Column Address (HEX)

COM Outputs

Row Address (HEX)

(Display Startline=0)

Nibble Re-map A[1]=0

Table 5 - GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, Display Start line=00H (Data byte sequence: D0, D1, D2 … D8191)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		3F		3E			01		00	
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]
|	|								
COM126	7E	D8127[7:4]	D8127[3:0]	D8126[7:4]	D8126[3:0]		D8065[7:4]	D8065[3:0]	D8064[7:4]	D8064[3:0]
COM127	7F	D8191[7:4]	D8191[3:0]	D8190[7:4]	D8190[3:0]		D8129[7:4]	D8129[3:0]	D8128[7:4]	D8128[3:0]

SEG Outputs

Column Address (HEX)

COM Outputs

Row Address (HEX)

(Display Startline=0)

Nibble Re-map A[1]=1

Table 6 - GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, Display Start Line=78H (Data byte sequence: D0, D1, D2 … D8191)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM118	01	D1[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
|	|								
COM121	7E	D126[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM120	7F	D127[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=78H)

Nibble Re-map A[1]=0

Table 7 - GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 … D7811), Column Start Address = 01H, Column End Address = 3EH, Row Start Address = 01H, Row End Address = 7EH

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00									
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]		
|	|								
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]		
COM127	7F									

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=0)

Nibble Re-map A[1]=0

Gray Scale Decoder

In SSD1328, there are 16 gray levels from GS0 to GS15. The gray scale of the display is defined by the pulse width (PW) of current drive phase, except GS0 there is no pre-charge and current drive. Each L value represents an offset to the corresponding gray scale level. See below table and graphical representation:

Table 8 -gray scale pulse width set table

	Description	Number of DCLKs
L1	Set GS1 level Pulse Width	0-7
L2	Set GS2 level Pulse Width Offset	1-8
L3	Set GS3 level Pulse Width Offset	1-8
.	.	.
.	.	.
.	.	.
L13	Set GS13 level Pulse Width Offset	1-8
L14	Set GS14 level Pulse Width Offset	1-8
L15	Set GS15 level Pulse Width Offset	1-8

DCLK: Internal Display Clock. It is used for defining phase clock period.

Figure 6 - Gray scale pulse width set diagram

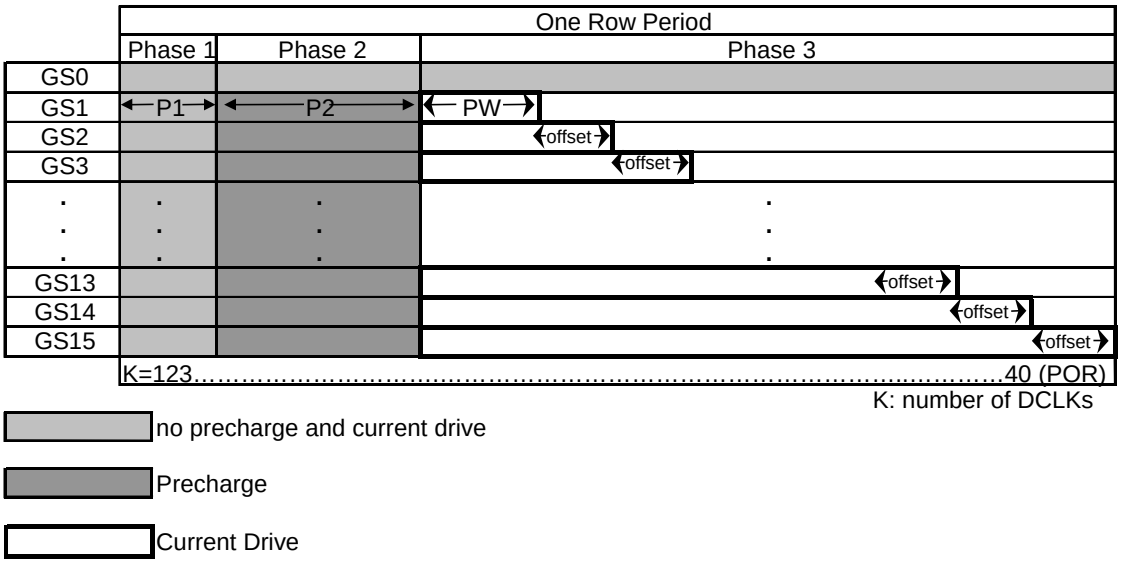


Table 9 - Gray scale pulse width default values

POR	Result
L1=1	GS1 level Pulse width=1
L2=1	GS2 level Pulse width=3
L3=1	GS3 level Pulse width=5
L4=1	GS4 level Pulse width=7
L5=1	GS5 level Pulse width=9
L6=1	GS6 level Pulse width=11
L7=1	GS7 level Pulse width=13
L8=1	GS8 level Pulse width=15
L9=1	GS9 level Pulse width=17
L10=1	GS10 level Pulse width=19
L11=1	GS11 level Pulse width=21
L12=1	GS12 level Pulse width=23
L13=1	GS13 level Pulse width=25
L14=1	GS14 level Pulse width=27
L15=1	GS15 level Pulse width=29

COMMAND TABLE

Table 10 - Command Table (D/C# =0, R/W#(WR#)=0, E (RD#)=1)

Hex	Command	Description
15 A[5:0] B[5:0]	Set Column Address	Second command A[5:0] sets the column start address from 0-63, POR=00H. Third command B[5:0] sets the column end address from 0-63, POR=3FH.
75 A[6:0] B[6:0]	Set Row address	Second command A[6:0]sets the row start address from 0-127, POR=00H. Third command B[6:0] sets the row end address from 0-127, POR=7FH.
81 A[6:0]	Set Contrast Control Register	Double byte command to select 1 out of 128 contrast steps. Contrast increases as level increase. The level is set to 40H after POR
84~86	Set Current Range	84H=Quarter Current Range (POR) 85H=Half Current Range 86H=Full Current Range
A0 A[6:0]	Set Re-map	A[0]=0, Disable Column Address Re-map (POR) A[0]=1, Enable Column Address Re-map A[1]=0, Disable Nibble Re-map (POR) A[1]=1, Enable Nibble Re-map A[2]=0, Disable Horizontal Address Increment (POR) A[2]=1, Enable Vertical Address Increment A[4]=0, Disable COM Re-map (POR) A[4]=1, Enable COM Re-map A[5]=0, Reserved (POR) A[5]=1, Reserved A[6]=0, Disable COM Split Odd Even (POR) A[6]=1, Enable COM Split Odd Even
A1 A[6:0]	Set Display Start Line	Set display RAM display start line register from 0-127. Display start line register is reset to 00H after POR.
A2 A[6:0]	Set Display Offset	Set vertical scroll by COM from 0-127. The value is reset to 00H after POR.
A4~A7	Set Display Mode	A4H=Normal Display (POR) A5H=Entire Display On, all pixels are turned on in GS level 15 A6H=Entire Display Off, all pixels turns off A7H=Inverse Display
A8 A[6:0]	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-128MUX, POR=7FH(128MUX)
AD A[7:0]	Initialization	The next command 02H must be issued after reset

AE~AF	Set Display On/Off	AEH=Display off (Sleep mode) (POR) AFH=Display on
B1 A[3:0] A[7:4]	Set Phase Length	A[3:0]=P1, phase 1 period of 1-16 DCLK clocks, POR=4 A[7:4]=P2, phase 2 period of 1-16 DCLK clocks, POR=7
B2 A[7:0]	Set Row Period	The next command sets the number of DCLKs, K, per row between 18-255, POR=40d display clocks The K value should be set as K=P1+P2+GS15 pulse width (POR: 4+7+29)
B3 A[3:0] A[7:4]	Set Display Clock Divide Ratio/Oscillator Frequency	The lower nibble of the next command sets the divide ratio of the display clocks: Divide ratio= 1-16, POR=1 The higher nibble of the next command sets the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa. POR=0
B8 A[2:0] B[2:0] B[6:4] C[2:0] C[6:4] D[2:0] D[6:4] E[2:0] E[6:4] F[2:0] F[6:4] G[2:0] G[6:4] H[2:0] H[6:4]	Set Gray Scale Table	The next eight bytes of command set the gray scale level of GS1-15 as below: A[2:0]=L1, POR=1 B[2:0]=L2, POR=1 B[6:4]=L3, POR=1 C[2:0]=L4 POR=1 C[6:4]=L5, POR=1 D[2:0]=L6, POR=1 D[6:4]=L7, POR=1 E[2:0]=L8, POR=1 E[6:4]=L9, POR=1 F[2:0]=L10, POR=1 F[6:4]=L11, POR=1 G[2:0]=L12, POR=1 G[6:4]=L13, POR=1 H[2:0]=L14, POR=1 H[6:4]=L15, POR=1
E3	NOP	Command for No Operation

Table 11 - Read Command Table (D/C#=0, R/W#(WR#)=1, E(RD#)=1 for 6800 or E(RD#)=0 for 8080)

$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D7=0:reserved D7=1:reserved D6=0:indicates the display is ON D6=1:indicated the display is OFF D5=0:reserved D5=1:reserved D4=0:reserved D4=1:reserved

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command;
Otherwise, unexpected result will occur

Data Read / Write

To read data from the GDDRAM, input High to R/W#(WR#) pin and D/C# pin for 6800-series parallel mode, Low to E (RD#) pin and High to D/C# pin for 8080-series parallel mode.

In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data read. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/W#(WR#) pin and High to D/C# pin for 6800-series parallel mode and 8080-series parallel mode. For serial interface mode, it is always in write mode. In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data write. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data write.

It should be noted that, in horizontal address increment mode, the row address pointer would be increased by one automatically if the column address pointer wraps around. In vertical address increment mode, the column address pointer will be increased by one automatically if the row address pointer wraps around.

D/C#	R/W#(WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

Table 12 - Address Increment Table (Automatic)

COMMAND DESCRIPTIONS

Set Column Address

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address.

Set Row Address

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address.

Set Contrast Control Register

This command is to set Contrast Setting of the display. The chip has 128 contrast steps from 00H to 7FH. The segment output current increases linearly with the increase of contrast step. See Figure 7 at below.

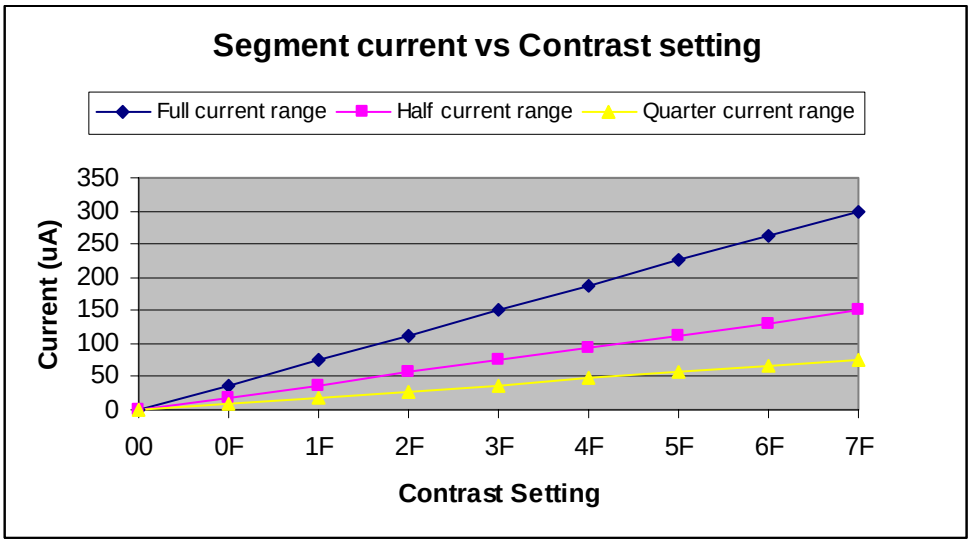


Figure 7 - Segment current vs Contrast setting

Set Current Range

This command is used to select quarter range or half range or full range current mode. With the same contrast level, quarter range mode will give a quarter of the current output of the full range mode. Similar to half range current mode, it will give a half of the current output of the full range mode. See Figure 7 for details. In POR, quarter range current mode is default.

Set Re-map

This command changes the mapping between the display data column address and segment driver, row address and common driver. It allows flexibility in layout during OLED module assembly. See the Re-map setting below:

Column Address Re-map

If column address re-map is set, Col 0-63 map to SEG127-0, regardless of start column and end column commands.

Nibble Re-map

If nibble re-map is set, the two nibbles of the data bus for RAM access are re-mapped, such that (D7, D6, D5, D4, D3, D2, D1, D0) acts like (D3, D2, D1, D0, D7, D6, D5, D4)
This feature working with Column Address Re-map would produce an effect of flipping outputs SEG0-127 to SEG127-SEG0.

Address Increment Mode

If horizontal increment mode is set, the column address pointer advances after each RAM access.
If vertical increment mode is set, the row address pointer advances after each RAM access.

COM Re-map

This 3-bit command is used to set the mapping for COM signals. If COM re-map is set, ROW 0-127 maps to COM127-0, regardless of start and end row commands. If COM split odd even is set, ROW0,2,4,…,62 map to COM0-63, ROW1,3,5,…,63 map to COM64-127. See Table 13 below:

A[4:6]	**COM 0-127**	
000	ROW 0-127	
100	ROW 127-0	
A[4:6]	**COM0,1,2,…,63**	**COM64,65,66,…,127**
000	ROW0,1,2,…,63	ROW64,65,66,…,127
001	ROW0,2,4,…,126	ROW1,3,5,…,127

Table 13 - COM Re-map setting

Set Display Start Line

This command is to set **Display Start Line** register to determine starting address of display RAM to be displayed by selecting a value from 0 to 127.

Set Display Offset

This is a double byte command. The next command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-127. For example, to move the COM16 towards the COM0 direction for 16 lines, the 7-bit data in the second command should be given by 0010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (128-16) and so the second command should be 1110000.

Set Display Mode

This command is used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display. Set Entire Display On forces the entire display to be at gray level “GS15” regardless of the contents of the display data RAM. Set Entire Display Off forces the entire display to be at gray level “GS0” regardless of the contents of the display data RAM. Normal Display will turn the data to ON at the corresponding gray level. Inverse display will turn the data as follow:

Table 14 - Mapping of data with each gray scale level at different display mode

Data $D_{X4}D_{X3}D_{X2}D_{X1}$	Normal Display (A4H)	Entire Display On (A5H)	Entire Display Off (A6H)	Inverse Display (A7H)
0000	GS0	GS15	GS0	GS15
0001	GS1	GS15	GS0	GS14
0010	GS2	GS15	GS0	GS13
0011	GS3	GS15	GS0	GS12
0100	GS4	GS15	GS0	GS11
0101	GS5	GS15	GS0	GS10
0110	GS6	GS15	GS0	GS9
0111	GS7	GS15	GS0	GS8
1000	GS8	GS15	GS0	GS7
1001	GS9	GS15	GS0	GS6
1010	GS10	GS15	GS0	GS5
1011	GS11	GS15	GS0	GS4
1100	GS12	GS15	GS0	GS3
1101	GS13	GS15	GS0	GS2
1110	GS14	GS15	GS0	GS1
1111	GS15	GS15	GS0	GS0

Set Multiplex Ratio

This command sets multiplex ratio from 16 to 128. In POR, multiplex ratio is 128.

Set Display On/Off

This command turns the display on or off. When the display is off, the segment and common output are in high impedance state.

Set Phase Length

This is a double byte command. The lower nibble of the second byte selects phase 1 period (no pre-charge and current drive) from 1 to 16 DCLKs. POR is A[3:0]=4. The higher nibble of the second byte is used to select phase 2 period (pre-charge) from 1 to 16 DCLKs. POR is A[7:4]=7.

Set Row Period

This command is used to set the row period. It is defined by multiplying the internal display clock period by the number of internal display clocks per row (Value from 18-255d). POR is 40d. The larger the value, the more precise of each gray scale level can be tuned. See “Gray Scale Table” command for details. Also, It is used to define the frame frequency with the use of “Display Clock Divide Ratio” command together.

Row period equals to the sum of phase 1, 2 periods and the pulse width of GS15. See equation in command table on page 20.

Set Display Clock Divide Ratio

This command is used to set the frequency of the internal display clocks, DCLKs. It is defined by dividing the oscillator frequency by the divide ratio (Value from 1 to 16). POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency. See equation on page 20.

Set Oscillator Frequency

This is a double byte command. The lower nibble of the second byte is used to select the oscillator frequency. Default value is shown in Table 17 on page 28.

Set Gray Scale Table

This command is used to set the gray scale table for the display. Except GS0, which has no pre-charge and current drive, each GS level is programmed by a set of offset values. As shown in Table 8, GS1 is defined with pulse width equals to the first offset value, L1, select from 0-7 internal display clocks. GS2 is defined with pulse width equals to GS1 plus the next offset value, L2, select from1-8 internal display clocks. Similarly, the next GS level is defined with pulse width equals to its lower one GS level plus the next offset value, select from 1-8 internal display clocks. In normal operation, GS15 should take the full current drive period as its pulse width. Therefore, the row period should be set as the sum of phase 1 period, phase 2 period, and the pulse width of GS15 with the use of “Row period” command.

NOP

No Operation Command.

Status register Read

This command is issued by setting D/C# low during a data read (refer to Figure 8 and Figure 9 parallel interface waveform). It allows the MCU to monitor the internal status of the chip.

MAXIMUM RATINGS

Table 15 - Maximum Ratings (Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{CC}		0 to 18	V
V_{REF}		0 to 18	V
V_{COMH}	Supply Voltage/Output voltage	0 to 16	V
-	SEG/COM output voltage	0 to 16	V
V_{in}	Input voltage	Vss-0.3 to Vdd+0.3	V
T_A	Operating Temperature	-30 to +90	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

DC CHARACTERISTICS

Table 16 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25ºC)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	8	12	18	V
V_{DD}	Logic Supply Voltage	-	2.4	2.7	3.5	V
V_{OH}	High Logic Output Level	IOUT = 100uA, 3.3MHz	0.9*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	IOUT = 100uA, 3.3MHz	0	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	IOUT = 100uA, 3.3MHz	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	IOUT = 100uA, 3.3MHz	0	-	0.2*V_{DD}	V
I_{SLEEP}	Sleep mode Current	No loading	-	0.2	5	uA
I_{CC}	V_{CC} Supply Current VDD=2.7V, external VCC=12V, IREF=10uA, Frame rate=110Hz, All one pattern, Display on, no loading	Contrast = 7F	-	-	850	uA
I_{DD}	V_{DD} Supply Current VDD=2.7V, external VCC=12V, IREF=10uA, Frame rate=110Hz, All one pattern, Display on, no loading	Contrast = 7F	-	-	200	uA
I_{SEG}	Segment Output Current VDD=2.7V, VCC=12V, IREF=10uA, Frame rate=110Hz, Display on, Segment pin under test is connected with a 20K resistive load to VSS	Contrast = 7F	250	300	370	uA
		Contrast = 5F	-	225	-	
		Contrast = 3F	-	150	-	
		Contrast = 1F	50	75	100	
Dev	Segment output current uniformity V_{DD}=2.7V, V_{CC}=12V, I_{REF}=10uA, Contrast=7F	Adjacent pin	-	±2	-	%
		Overall pin to pin	-	-	±3	

AC CHARACTERISTICS

Table 17 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	Vdd = 2.7V, IREF = 10uA	530	585	630	kHz
F_{FRM}	Frame Frequency for 128 MUX Mode	128x128 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} X 1/(D*K*128)	-	Hz

D: divide ratio
K: number of display clocks
Refer to command table for detail description

Table 18 - 6800-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

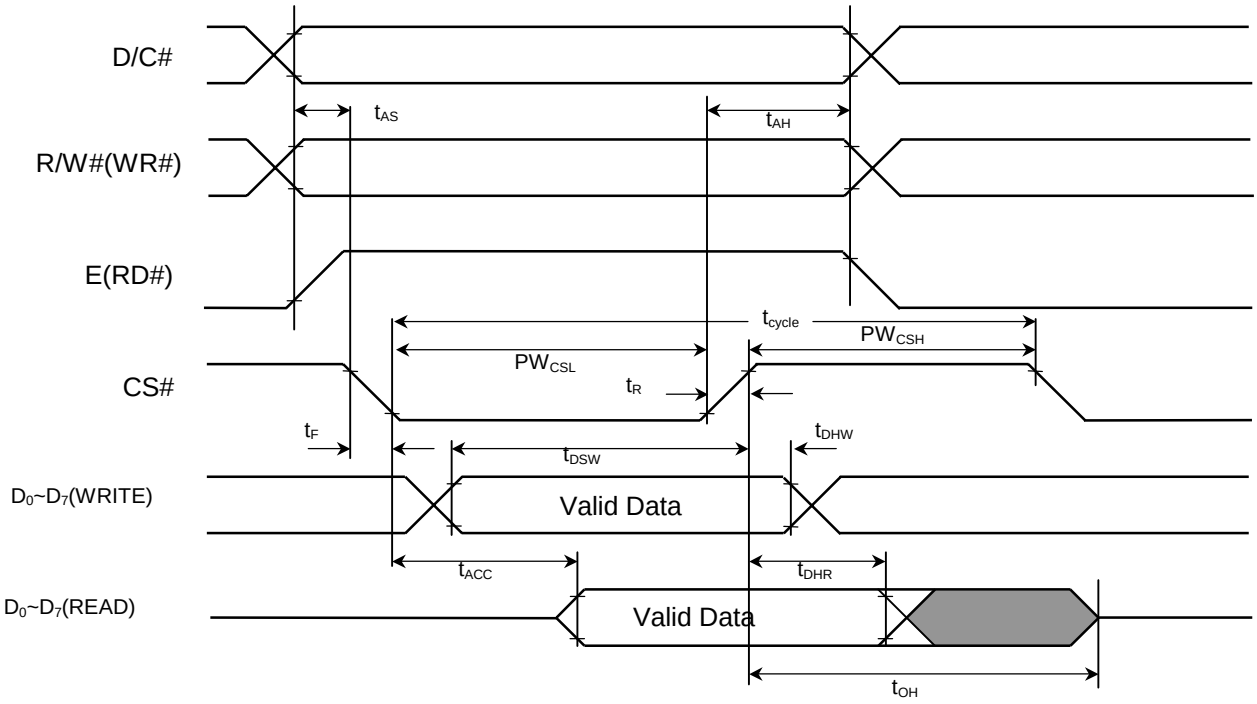


Figure 8 - 6800-series MPU Parallel Interface Characteristics

Table 19 - 8080-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

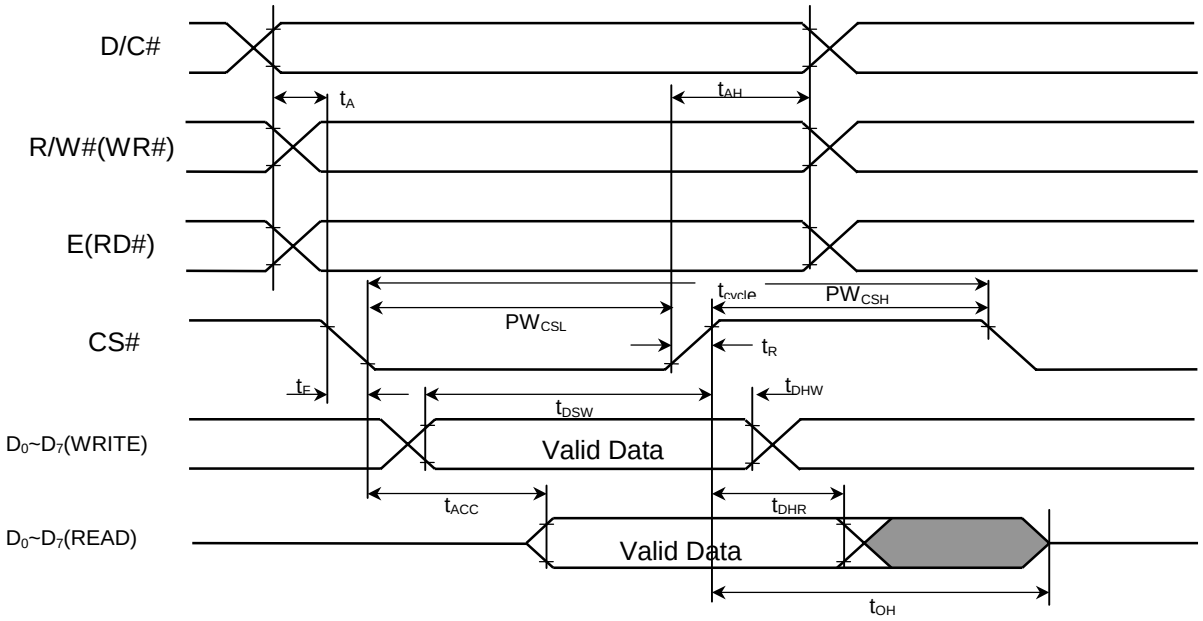


Figure 9 - 8080-series MPU Parallel Interface Characteristics

Table 20 - Serial Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

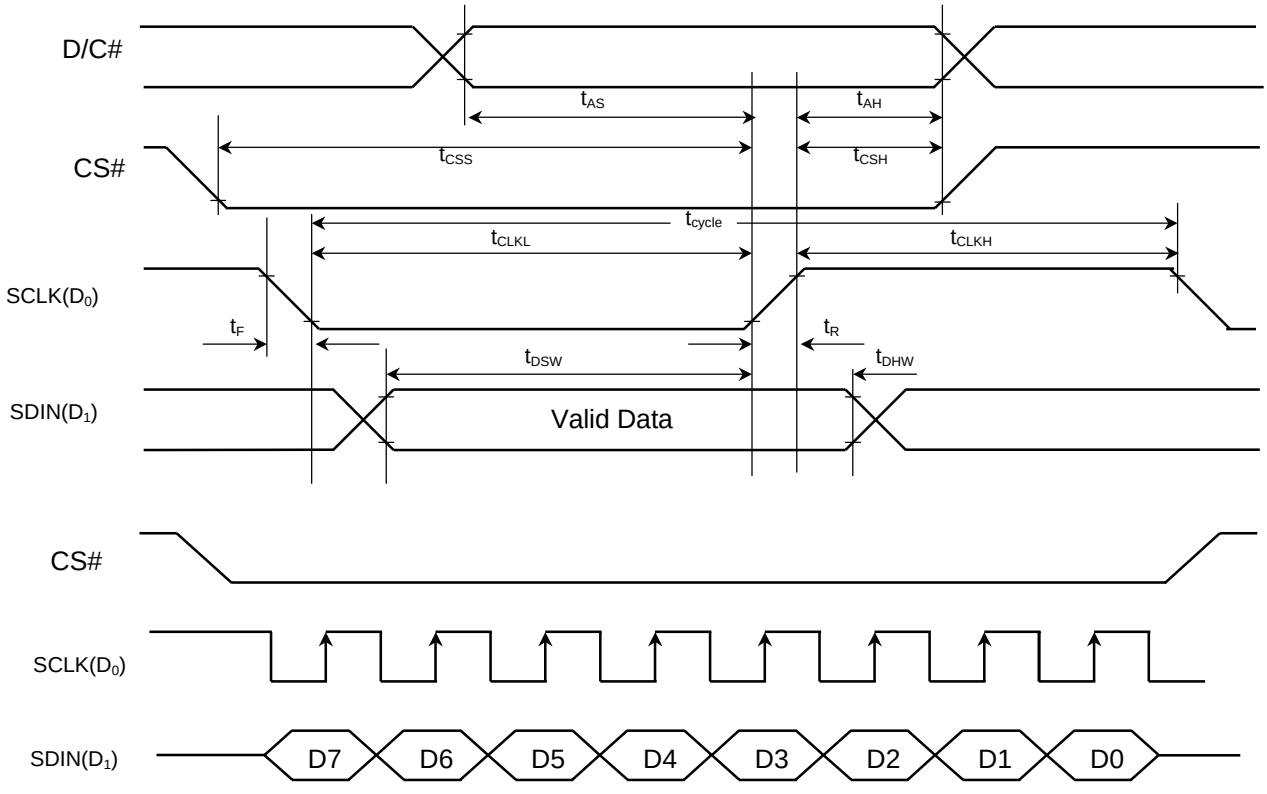
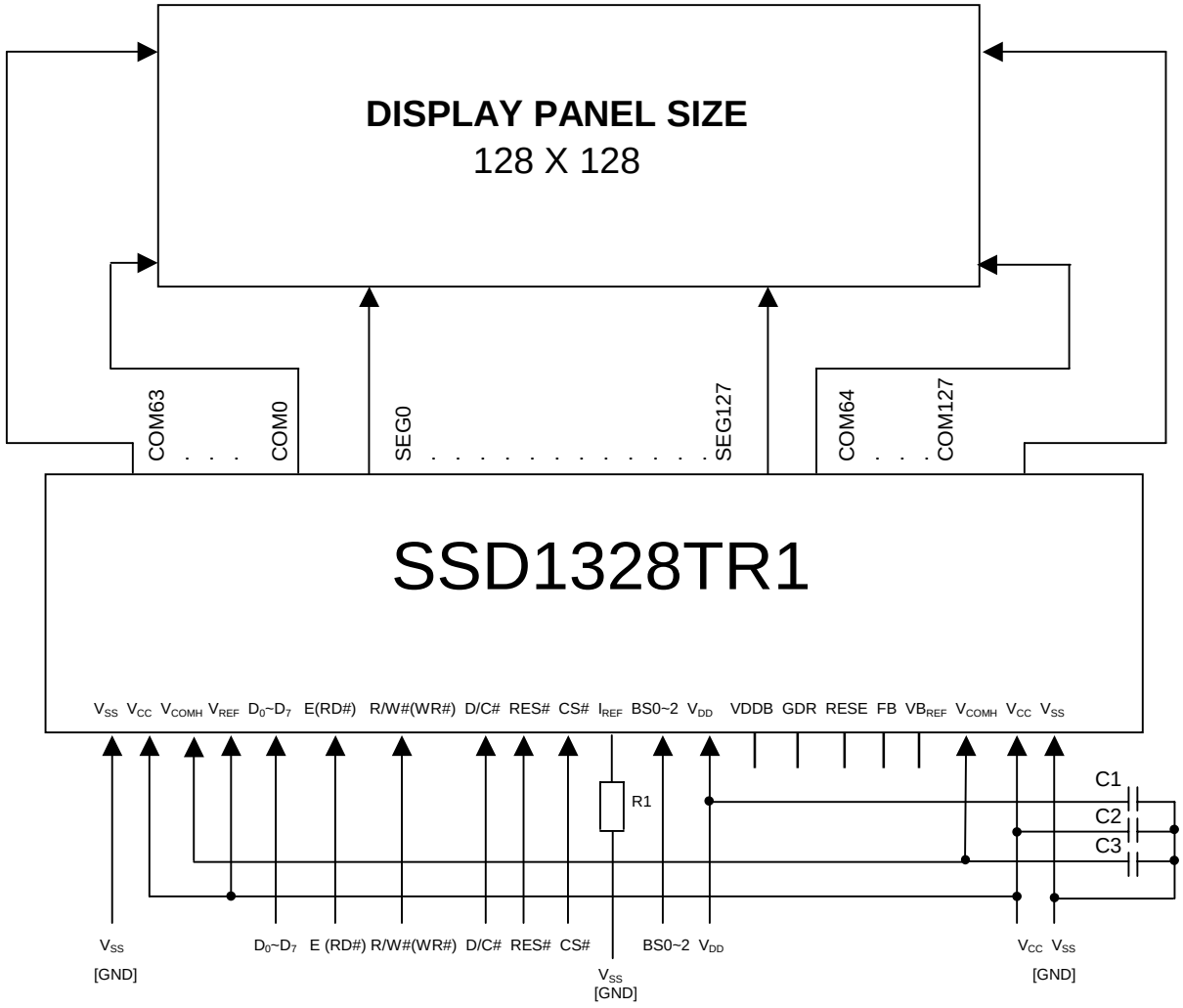


Figure 10 - Serial Interface Characteristics

APPLICATION EXAMPLE

The configuration for 6800-parallel interface mode, externally V_{CC} is shown in the following diagram: (V_{DD}=2.7V, V_{CC}=V_{REF}=12V, I_{REF}=10uA)

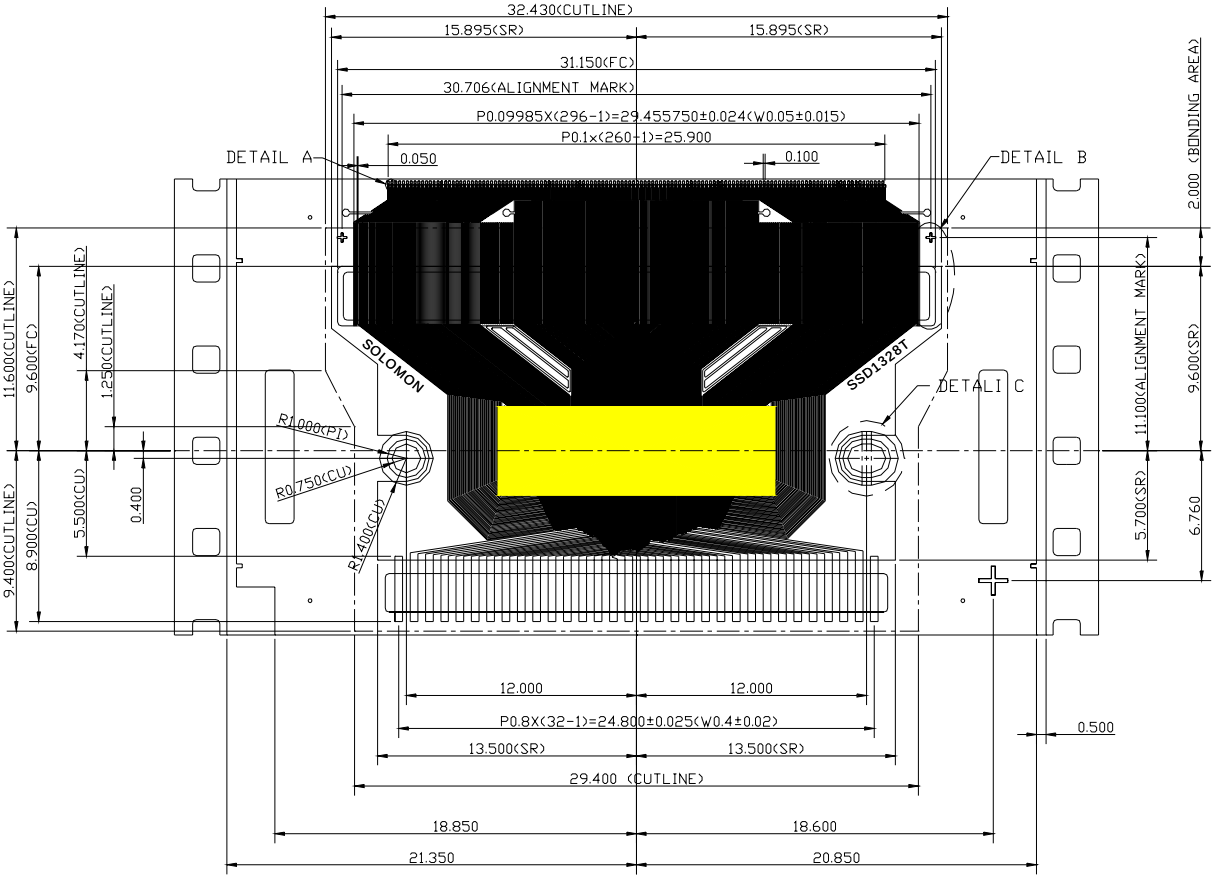


Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, CS#, RES#
Pin internally connected to VDD: M/S#, CLS
Pin internally connected to VSS: VSSB
Pin externally connected to VDD: BS2, VDDB
Pin externally connected to VSS: BS0, BS1
Pin externally connected to VCC: VREF
Pin floated: GDR, RESE, FB, VB_{REF}

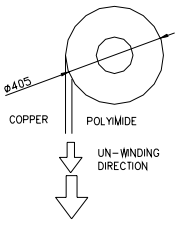
C1~ C3: 4.7uF
R1: 910kΩ, R1=(Voltage at IREF pin-VSS)/I_{REF}

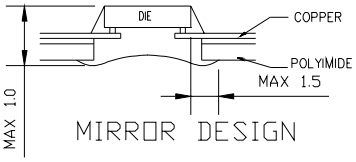
Figure 11 - Application Example for SSD1328TR1

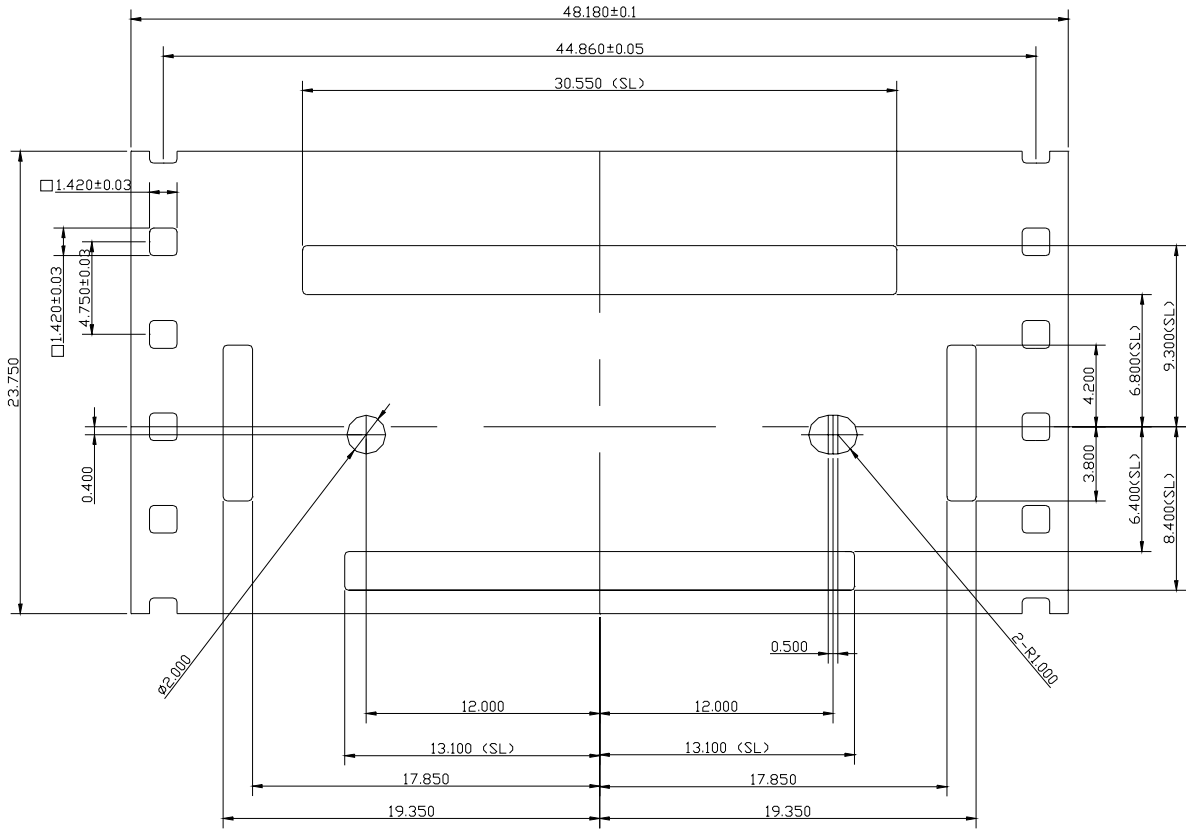
SSD1328TR1 TAB PACKAGE DIMENSION

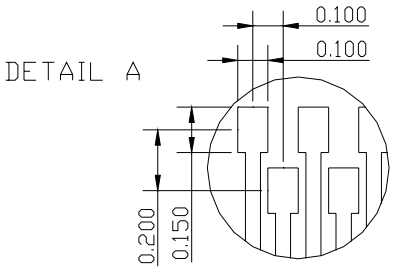


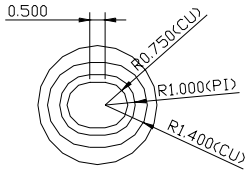
NOTE:
1. GENERAL TOLERANCE: ±0.05MM
2. MATERIAL
   PI: 75±6UM
   ADHESIVE: 12±2UM
   CU: 18±5UM
   SR: 26±14UM
   FLEX COATING: Max 0.7MM
   Thickness:Min 10UM
3. SN PLATING: 0.2±0.05UM
4. TAPSITE: 5 SPH, 23.75MM



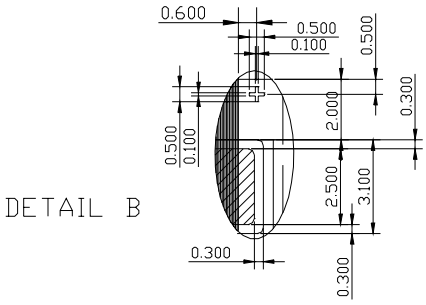



48.180±0.1
44.860±0.05
30.550 (SL)
□1.420±0.03
□1.420±0.03
4.750±0.03
23.750
0.400
4.200
6.800(SL)
9.300(SL)
3.800
6.400(SL)
8.400(SL)
ø2.000
0.500
2-R1.000
12.000
12.000
13.100 (SL)
13.100 (SL)
17.850
17.850
19.350
19.350

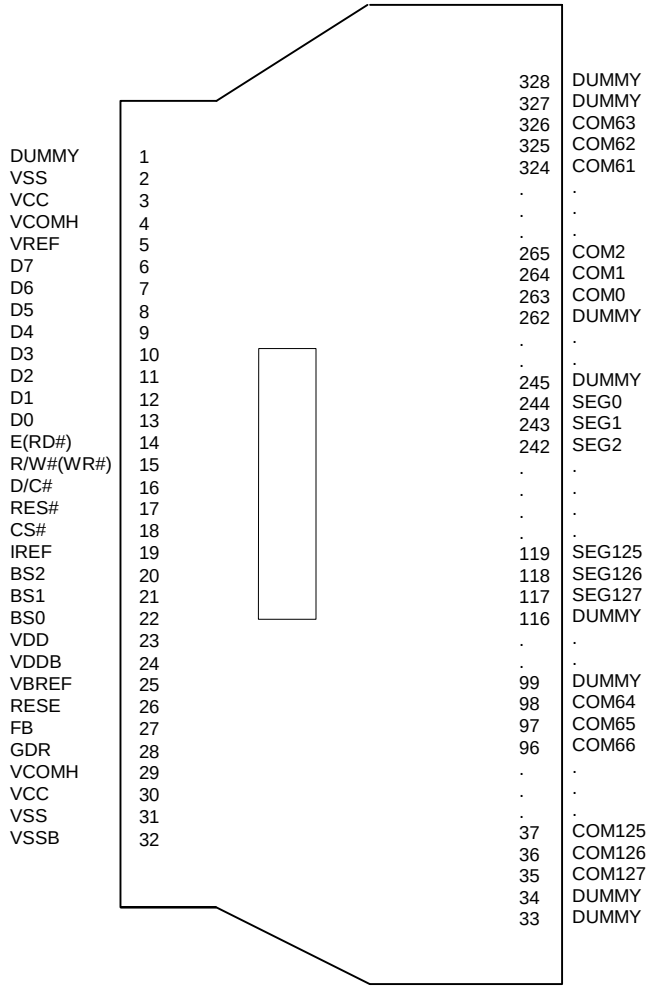

DETAIL A
0.100
0.100
0.200
0.150

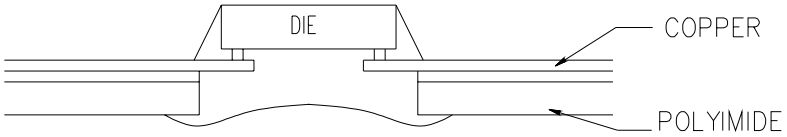

0.500
R0.750(CU)
R1.000(PI)
R1.400(CU)

DETAIL C


DETAIL B
0.600
0.500
0.100
0.500
0.500
0.100
2.000
0.300
2.500
3.100
0.300
0.300

SSD1328TR1 PIN ASSIGNMENT





MIRROR DESIGN

Figure 12 - SSD1328TR1 TAB pin assignment (Copper view, Mirror TAB design)

Note: Dummy pin should be in no connection and do not group them together.

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	DUMMY	33	DUMMY	99	DUMMY	149	SEG95	213	SEG31	263	COM0
2	VSS	34	DUMMY	100	DUMMY	150	SEG94	214	SEG30	264	COM1
3	VCC	35	COM127	101	DUMMY	151	SEG93	215	SEG29	265	COM2
4	VCOMH	36	COM126	102	DUMMY	152	SEG92	216	SEG28	266	COM3
5	VREF	37	COM125	103	DUMMY	153	SEG91	217	SEG27	267	COM4
6	D7	38	COM124	104	DUMMY	154	SEG90	218	SEG26	268	COM5
7	D6	39	COM123	105	DUMMY	155	SEG89	219	SEG25	269	COM6
8	D5	40	COM122	106	DUMMY	156	SEG88	220	SEG24	270	COM7
9	D4	41	COM121	107	DUMMY	157	SEG87	221	SEG23	271	COM8
10	D3	42	COM120	108	DUMMY	158	SEG86	222	SEG22	272	COM9
11	D2	43	COM119	109	DUMMY	159	SEG85	223	SEG21	273	COM10
12	D1	44	COM118	110	DUMMY	160	SEG84	224	SEG20	274	COM11
13	D0	45	COM117	111	DUMMY	161	SEG83	225	SEG19	275	COM12
14	E(RD#)	46	COM116	112	DUMMY	162	SEG82	226	SEG18	276	COM13
15	R/W#(WR#)	47	COM115	113	DUMMY	163	SEG81	227	SEG17	277	COM14
16	D/C#	48	COM114	114	DUMMY	164	SEG80	228	SEG16	278	COM15
17	RES#	49	COM113	115	DUMMY	165	SEG79	229	SEG15	279	COM16
18	CS#	50	COM112	116	DUMMY	166	SEG78	230	SEG14	280	COM17
19	IREF	51	COM111	117	SEG127	167	SEG77	231	SEG13	281	COM18
20	BS2	52	COM110	118	SEG126	168	SEG76	232	SEG12	282	COM19
21	BS1	53	COM109	119	SEG125	169	SEG75	233	SEG11	283	COM20
22	BS0	54	COM108	120	SEG124	170	SEG74	234	SEG10	284	COM21
23	VDD	55	COM107	121	SEG123	171	SEG73	235	SEG9	285	COM22
24	VDDB	56	COM106	122	SEG122	172	SEG72	236	SEG8	286	COM23
25	VBREF	57	COM105	123	SEG121	173	SEG71	237	SEG7	287	COM24
26	RESE	58	COM104	124	SEG120	174	SEG70	238	SEG6	288	COM25
27	FB	59	COM103	125	SEG119	175	SEG69	239	SEG5	289	COM26
28	GDR	60	COM102	126	SEG118	176	SEG68	240	SEG4	290	COM27
29	VCOMH	61	COM101	127	SEG117	177	SEG67	241	SEG3	291	COM28
30	VCC	62	COM100	128	SEG116	178	SEG66	242	SEG2	292	COM29
31	VSS	63	COM99	129	SEG115	179	SEG65	243	SEG1	293	COM30
32	VSSB	64	COM98	130	SEG114	180	SEG64	244	SEG0	294	COM31
		65	COM97	131	SEG113	181	SEG63	245	DUMMY	295	COM32
		66	COM96	132	SEG112	182	SEG62	246	DUMMY	296	COM33
		67	COM95	133	SEG111	183	SEG61	247	DUMMY	297	COM34
		68	COM94	134	SEG110	184	SEG60	248	DUMMY	298	COM35
		69	COM93	135	SEG109	185	SEG59	249	DUMMY	299	COM36
		70	COM92	136	SEG108	186	SEG58	250	DUMMY	300	COM37
		71	COM91	137	SEG107	187	SEG57	251	DUMMY	301	COM38
		72	COM90	138	SEG106	188	SEG56	252	DUMMY	302	COM39
		73	COM89	139	SEG105	189	SEG55	253	DUMMY	303	COM40
		74	COM88	140	SEG104	190	SEG54	254	DUMMY	304	COM41
		75	COM87	141	SEG103	191	SEG53	255	DUMMY	305	COM42
		76	COM86	142	SEG102	192	SEG52	256	DUMMY	306	COM43
		77	COM85	143	SEG101	193	SEG51	257	DUMMY	307	COM44
		78	COM84	144	SEG100	194	SEG50	258	DUMMY	308	COM45
		79	COM83	145	SEG99	195	SEG49	259	DUMMY	309	COM46
		80	COM82	146	SEG98	196	SEG48	260	DUMMY	310	COM47
		81	COM81	147	SEG97	197	SEG47	261	DUMMY	311	COM48
		82	COM80	148	SEG96	198	SEG46	262	DUMMY	312	COM49
		83	COM79			199	SEG45			313	COM50
		84	COM78			200	SEG44			314	COM51
		85	COM77			201	SEG43			315	COM52
		86	COM76			202	SEG42			316	COM53
		87	COM75			203	SEG41			317	COM54
		88	COM74			204	SEG40			318	COM55
		89	COM73			205	SEG39			319	COM56
		90	COM72			206	SEG38			320	COM57
		91	COM71			207	SEG37			321	COM58
		92	COM70			208	SEG36			322	COM59
		93	COM69			209	SEG35			323	COM60
		94	COM68			210	SEG34			324	COM61
		95	COM67			211	SEG33			325	COM62
		96	COM66			212	SEG32			326	COM63
		97	COM65							327	DUMMY
		98	COM64							328	DUMMY

Table 21 - SSD1328TR1 pin assignment

Appendix

Internal DC-DC Voltage Converter Application Circuit

It is a switching voltage generator circuit, designed for handheld applications. In SSD1328, internal DC-DC voltage converter accompanying with an external application circuit (shown in below figure) can generate a high voltage supply VCC from a low voltage supply input VDD. VCC is the voltage supply to the OLED driver block. Below application circuit is an example for the input voltage of 3V VDD to generate VCC of 12V @20mA ~ 30mA application. VCC out should be connected to Vcc pin of SSD1328 to provide the most positive voltage of the chip.

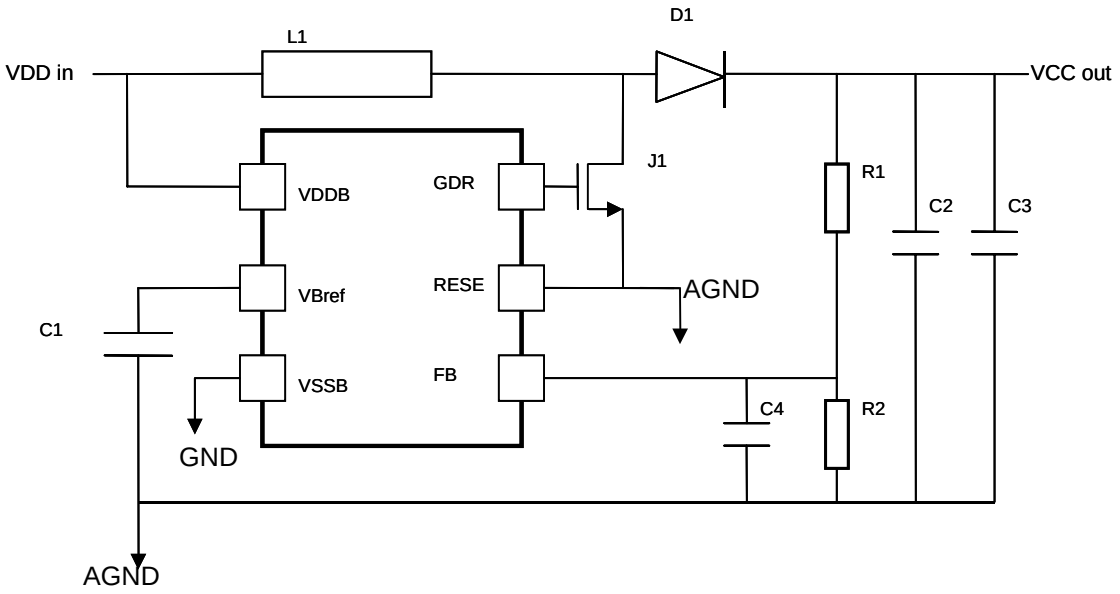


Figure 13- Application circuit diagram of SSD1328 internal DC-DC converter

Below is the pin description of internal DC-DC converter.

VDDB

This is the power supply pin for the internal buffer of the DC-DC voltage converter. It must be connected when the converter is used

VSSB

This is the GND pin for the internal buffer of the DC-DC voltage converter. It must be connected when the converter is used

GDR

This output pin drives the gate of the external NMOS of the booster circuit.

RESE

This pin connects to the source current pin of the external NMOS of the booster circuit

VB_{REF}

This pin is the internal voltage reference of booster circuit. A stabilization capacitor, typ. 1uF, should be connected to Vss.

FB

This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (Vcc).

Set DC-DC Converter Command

This command is used to enable or disable the internal DC-DC voltage converter. To enable the converter, send command 03H instead of 02H after command header ADH in the initialization after power on reset.

Hex	Command	Description
AD A[7:0]	Set DC-DC Converter	02H = Disable DC-DC converter. 03H = Enable DC-DC converter (POR).

Passive components selection:

Components	Typ. Value	Remark
L1	Inductor, 22µH	2A
D1	Schottky diode	2A, 25V e.g. 1N5822
J1	Power FET	N-FET with low rDS(on) and low Vth voltage. e.g. MGSF1N02LT1 [ON SEMICONDUCTOR]
R1, R2	Resistor, see below equation	1%,1/4W
C1	Capacitor, 1µF	16V
C2	Capacitor, 22µF	Low ESR, 25V
C3	Capacitor, 1µF	16V
C4	Capacitor, 0.01µF	16V

Table 22- Component lists for internal DC-DC converter application

The VCC output voltage level can be adjusted by R1 and R2, the reference formula is:

$$VCC = 1.2 \times (R1+R2) / R2$$

***All paths to AGND should be connected as short as possible**

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Vcc	DC-DC converter output voltage	VDD input=3V, L=22uH; R1=450Kohm; R2=50Kohm; Icc = 20mA(loading)	10	-	12	V
Pwr	DC-DC converter output power	VDD input=3V, L=22uH; Vcc = 12V	-	-	400	mW

http://www.solomon-systech.com