SSD1329

Product Preview

128 x 128 OLED Segment / Common Driver with Controller Equips with 16 Gray Scale Levels and 64 Hard Icon Lines

This document contains information on a product under development. Solomon Systech reserves the right to change or discontinue this product without notice.

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1329 is a single-chip CMOS OLED/PLED driver with controller for 16 gray scale levels organic / polymer light emitting diode dot-matrix graphic display system. SSD1329 consists of 128 segments, 128 commons and 64 hard icons. This IC is designed for Common Cathode type OLED / PLED panel.

SSD1329 displays data directly from its internal 128 x 128 x 4 bits Graphic Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface or Serial Peripheral Interface.

2 FEATURES

- Support max. 128 x 128 matrix panel
- Support 64 hard icons, 2 icon rows with 2 pins for each row
- Power supply: VDD = 2.4-3.5V
  VCI = 3.2-4.2V
  VDDIO = 1.7V - 3.5V (must be smaller than or equal to VDD)
  VCC = 9.0V - 18.0V
- For matrix display:
  - OLED driving output voltage, 16V maximum
  - Segment maximum source current: 300uA
  - Common maximum sink current: 40mA
  - Common R_{on} resistance: 20Ω
- For hard icons:
  - Segment maximum source current: 127.5uA
  - 128 steps current control
- DC-DC 2X voltage converter for hard icons
- Embedded 128 x 128 x 4 bit SRAM display buffer
- 256 steps contrast current control
- Internal oscillator
- Programmable frame rate
- Continuous horizontal and vertical scrolling
- 8-bit 6800-series Parallel Interface, 8080-series Parallel Interface and Serial Peripheral Interface.
- Wide range of operating temperature: -40 to 85 °C

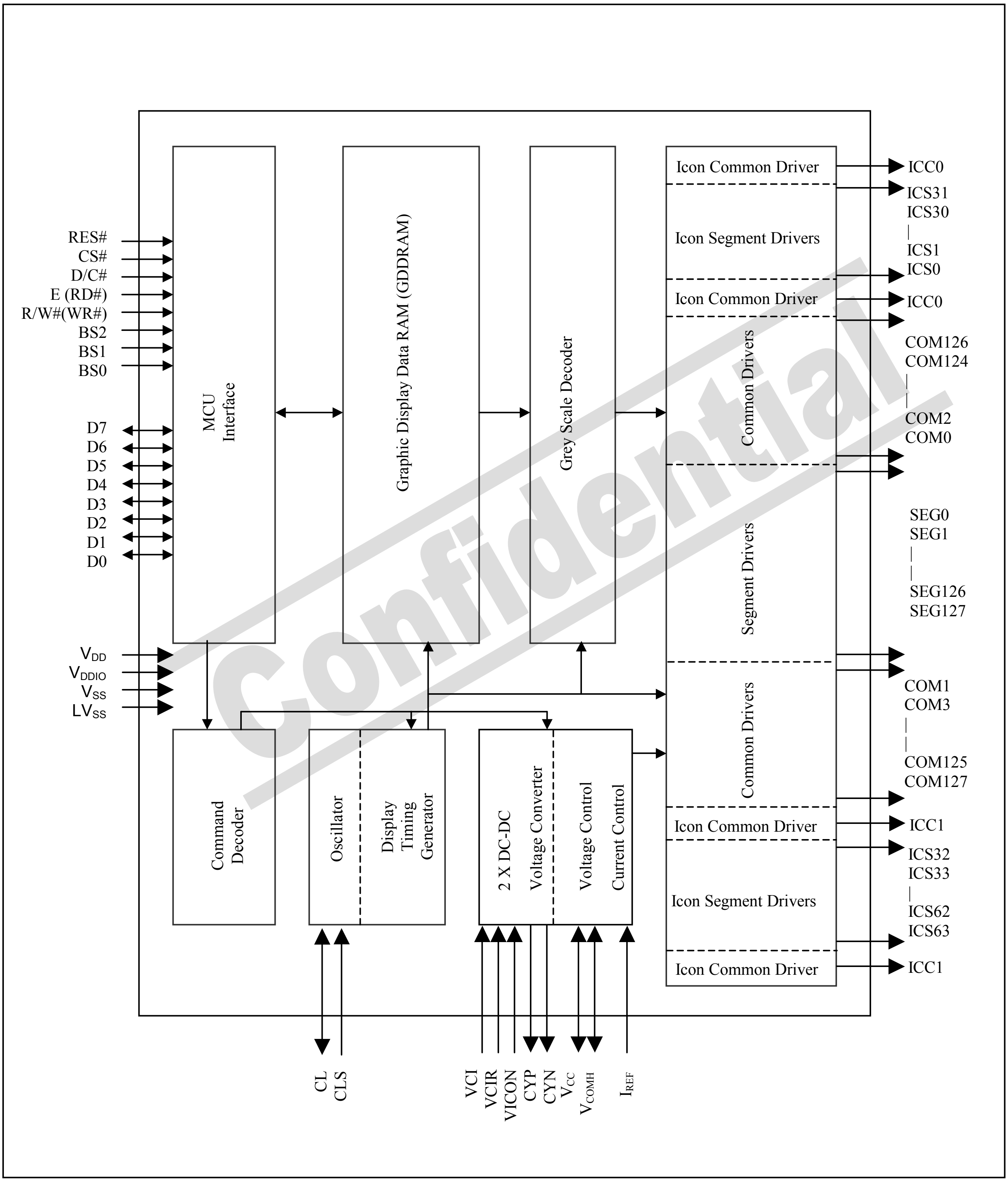
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	SEG	COM	Icon SEG	Icon COM	Package Form	Reference	Remark
SSD1329UR1	128	128	64	2	COF	Page 12, 54	• 48mm film • 5 sprocket hole • Folding COF • 80 / 68 / SPI interface • Output lead pitch: 71um
SSD1329Z	128	128	64	2	COG	Page 8	• Min SEG pad pitch: 43.2 um • Min COM pad pitch: 51.8 um
SSD1329U1	128	128	-	-	COF	Page 14, 55	• Punch out COF with stiffener • 80 / 68 / SPI interface • Output lead pitch: 0.1mm

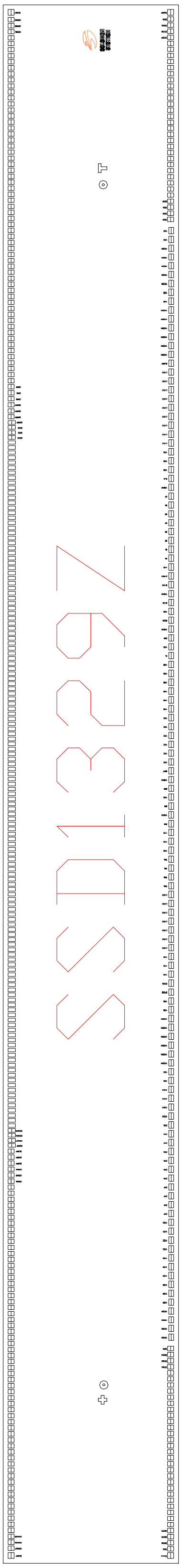
4 BLOCK DIAGRAM

Figure 4-1 : SSD1329 Block Diagram

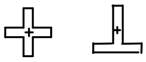


5 DIE PAD FLOOR PLAN

Figure 5-1 : SSD1329Z Die Drawing



← Pad #1



Note

[1] + represents the center of the alignment mark

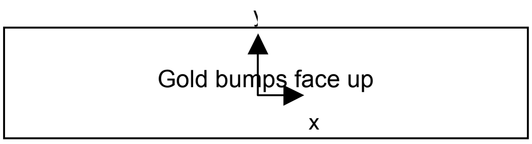
	X-Axis (um)	Y-Axis (um)
	+5300.0	-100.0
	-5300.0	-100.0

All alignment keys have size 75 um x 75 um

Die Size	13410 um x 1504 um
Die Thickness	457 um ± 25 um
Min I/O pad pitch	76.2 um
Min SEG pad pitch	43.2 um
Min COM pad pitch	51.8 um
Bump Height	Nominal 15 um

Bump Size

Pad #	**X [um]**	**Y [um]**
1, 196, 197, 477	50	52
2-35, 162-195	38	52
36-161	56	44
198-264, 410-476	38	52
265-409	31	64



Pad 1,2,3 …→

Figure 5-2 : SSD1329Z Alignment Mark Dimensions

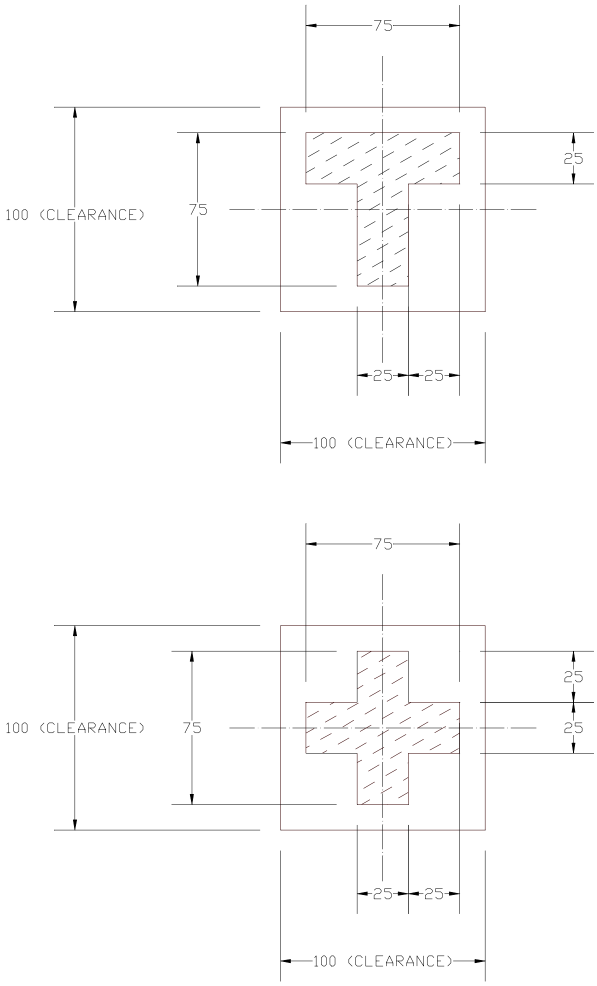


Table 5-1 : SSD1329Z Bump Die Pad Coordinates

Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis
1	DUMMY	-6640.0	-686.0	81	LVSS	-1333.5	-690.0	161	VCC	4762.5	-690.0	241	COM20	4349.8	686.0
2	ICC1	-6582.0	-686.0	82	LVSS	-1257.3	-690.0	162	ICC0	4859.4	-686.0	242	COM19	4298.0	686.0
3	ICS32	-6529.8	-686.0	83	LVSS	-1181.1	-690.0	163	ICS0	4911.6	-686.0	243	COM18	4246.2	686.0
4	ICS33	-6477.6	-686.0	84	LVSS	-1104.9	-690.0	164	ICS1	4963.8	-686.0	244	COM17	4194.4	686.0
5	ICS34	-6425.4	-686.0	85	LVSS	-1028.7	-690.0	165	ICS2	5016.0	-686.0	245	COM16	4142.6	686.0
6	ICS35	-6373.2	-686.0	86	LVSS	-952.5	-690.0	166	ICS3	5068.2	-686.0	246	COM15	4090.8	686.0
7	ICS36	-6321.0	-686.0	87	TR3	-876.3	-690.0	167	ICS4	5120.4	-686.0	247	COM14	4039.0	686.0
8	ICS37	-6268.8	-686.0	88	TR2	-800.1	-690.0	168	ICS5	5172.6	-686.0	248	COM13	3987.2	686.0
9	ICS38	-6216.6	-686.0	89	TR1	-723.9	-690.0	169	ICS6	5224.8	-686.0	249	COM12	3935.4	686.0
10	ICS39	-6164.4	-686.0	90	TR0	-647.7	-690.0	170	ICS7	5277.0	-686.0	250	COM11	3883.6	686.0
11	ICS40	-6112.2	-686.0	91	VSS	-571.5	-690.0	171	ICS8	5329.2	-686.0	251	COM10	3831.8	686.0
12	ICS41	-6060.0	-686.0	92	VSS	-495.3	-690.0	172	ICS9	5381.4	-686.0	252	COM9	3780.0	686.0
13	ICS42	-6007.8	-686.0	93	VSS	-419.1	-690.0	173	ICS10	5433.6	-686.0	253	COM8	3728.2	686.0
14	ICS43	-5955.6	-686.0	94	BS0	-342.9	-690.0	174	ICS11	5485.8	-686.0	254	COM7	3676.4	686.0
15	ICS44	-5903.4	-686.0	95	VDDIO	-266.7	-690.0	175	ICS12	5538.0	-686.0	255	COM6	3624.6	686.0
16	ICS45	-5851.2	-686.0	96	BS1	-190.5	-690.0	176	ICS13	5590.2	-686.0	256	COM5	3572.8	686.0
17	ICS46	-5799.0	-686.0	97	VSS	-114.3	-690.0	177	ICS14	5642.4	-686.0	257	COM4	3521.0	686.0
18	ICS47	-5746.8	-686.0	98	BS2	-38.1	-690.0	178	ICS15	5694.6	-686.0	258	COM3	3469.2	686.0
19	ICS48	-5694.6	-686.0	99	VDDIO	38.1	-690.0	179	ICS16	5746.8	-686.0	259	COM2	3417.4	686.0
20	ICS49	-5642.4	-686.0	100	IREF	114.3	-690.0	180	ICS17	5799.0	-686.0	260	COM1	3365.6	686.0
21	ICS50	-5590.2	-686.0	101	VCC	190.5	-690.0	181	ICS18	5851.2	-686.0	261	COM0	3313.8	686.0
22	ICS51	-5538.0	-686.0	102	VCC	266.7	-690.0	182	ICS19	5903.4	-686.0	262	DUMMY	3262.0	686.0
23	ICS52	-5485.8	-686.0	103	VCC	342.9	-690.0	183	ICS20	5955.6	-686.0	263	DUMMY	3210.2	686.0
24	ICS53	-5433.6	-686.0	104	VCC	419.1	-690.0	184	ICS21	6007.8	-686.0	264	DUMMY	3158.4	686.0
25	ICS54	-5381.4	-686.0	105	VCC	495.3	-690.0	185	ICS22	6060.0	-686.0	265	DUMMY	3110.4	680.0
26	ICS55	-5329.2	-686.0	106	VCC	571.5	-690.0	186	ICS23	6112.2	-686.0	266	SEG0	3067.2	680.0
27	ICS56	-5277.0	-686.0	107	VDD	647.7	-690.0	187	ICS24	6164.4	-686.0	267	SEG1	3024.0	680.0
28	ICS57	-5224.8	-686.0	108	VDD	723.9	-690.0	188	ICS25	6216.6	-686.0	268	SEG2	2980.8	680.0
29	ICS58	-5172.6	-686.0	109	VDD	800.1	-690.0	189	ICS26	6268.8	-686.0	269	SEG3	2937.6	680.0
30	ICS59	-5120.4	-686.0	110	VDD	876.3	-690.0	190	ICS27	6321.0	-686.0	270	SEG4	2894.4	680.0
31	ICS60	-5068.2	-686.0	111	VDD	952.5	-690.0	191	ICS28	6373.2	-686.0	271	SEG5	2851.2	680.0
32	ICS61	-5016.0	-686.0	112	VDD	1028.7	-690.0	192	ICS29	6425.4	-686.0	272	SEG6	2808.0	680.0
33	ICS62	-4963.8	-686.0	113	CL	1104.9	-690.0	193	ICS30	6477.6	-686.0	273	SEG7	2764.8	680.0
34	ICS63	-4911.6	-686.0	114	VSS	1181.1	-690.0	194	ICS31	6529.8	-686.0	274	SEG8	2721.6	680.0
35	ICC1	-4859.4	-686.0	115	CS#	1257.3	-690.0	195	ICC0	6582.0	-686.0	275	SEG9	2678.4	680.0
36	VICON	-4762.5	-690.0	116	VDDIO	1333.5	-690.0	196	DUMMY	6640.0	-686.0	276	SEG10	2635.2	680.0
37	VICON	-4686.3	-690.0	117	RES#	1409.7	-690.0	197	DUMMY	6640.0	686.0	277	SEG11	2592.0	680.0
38	VICON	-4610.1	-690.0	118	VSS	1485.9	-690.0	198	COM63	6577.2	686.0	278	SEG12	2548.8	680.0
39	VICON	-4533.9	-690.0	119	D/C#	1562.1	-690.0	199	COM62	6525.4	686.0	279	SEG13	2505.6	680.0
40	VCIR	-4457.7	-690.0	120	VDDIO	1638.3	-690.0	200	COM61	6473.6	686.0	280	SEG14	2462.4	680.0
41	VCIR	-4381.5	-690.0	121	R/W#	1714.5	-690.0	201	COM60	6421.8	686.0	281	SEG15	2419.2	680.0
42	VCIR	-4305.3	-690.0	122	E/RD#	1790.7	-690.0	202	COM59	6370.0	686.0	282	SEG16	2376.0	680.0
43	VCIR	-4229.1	-690.0	123	VSS	1866.9	-690.0	203	COM58	6318.2	686.0	283	SEG17	2332.8	680.0
44	VCIR	-4152.9	-690.0	124	D0	1943.1	-690.0	204	COM57	6266.4	686.0	284	SEG18	2289.6	680.0
45	VCIR	-4076.7	-690.0	125	D1	2019.3	-690.0	205	COM56	6214.6	686.0	285	SEG19	2246.4	680.0
46	VCI1	-4000.5	-690.0	126	D2	2095.5	-690.0	206	COM55	6162.8	686.0	286	SEG20	2203.2	680.0
47	VCI1	-3924.3	-690.0	127	D3	2171.7	-690.0	207	COM54	6111.0	686.0	287	SEG21	2160.0	680.0
48	VCI1	-3848.1	-690.0	128	D4	2247.9	-690.0	208	COM53	6059.2	686.0	288	SEG22	2116.8	680.0
49	VCI1	-3771.9	-690.0	129	D5	2324.1	-690.0	209	COM52	6007.4	686.0	289	SEG23	2073.6	680.0
50	CYP	-3695.7	-690.0	130	D6	2400.3	-690.0	210	COM51	5955.6	686.0	290	SEG24	2030.4	680.0
51	CYP	-3619.5	-690.0	131	D7	2476.5	-690.0	211	COM50	5903.8	686.0	291	SEG25	1987.2	680.0
52	CYP	-3543.3	-690.0	132	VDDIO	2552.7	-690.0	212	COM49	5852.0	686.0	292	SEG26	1944.0	680.0
53	CYP	-3467.1	-690.0	133	CLS	2628.9	-690.0	213	COM48	5800.2	686.0	293	SEG27	1900.8	680.0
54	CYN	-3390.9	-690.0	134	VSS	2705.1	-690.0	214	COM47	5748.4	686.0	294	SEG28	1857.6	680.0
55	CYN	-3314.7	-690.0	135	VSS	2781.3	-690.0	215	COM46	5696.6	686.0	295	SEG29	1814.4	680.0
56	CYN	-3238.5	-690.0	136	VSS	2857.5	-690.0	216	COM45	5644.8	686.0	296	SEG30	1771.2	680.0
57	CYN	-3162.3	-690.0	137	LVSS	2933.7	-690.0	217	COM44	5593.0	686.0	297	SEG31	1728.0	680.0
58	CYN	-3086.1	-690.0	138	LVSS	3009.9	-690.0	218	COM43	5541.2	686.0	298	SEG32	1684.8	680.0
59	CYN	-3009.9	-690.0	139	LVSS	3086.1	-690.0	219	COM42	5489.4	686.0	299	SEG33	1641.6	680.0
60	CYN	-2933.7	-690.0	140	LVSS	3162.3	-690.0	220	COM41	5437.6	686.0	300	SEG34	1598.4	680.0
61	VCHS	-2857.5	-690.0	141	LVSS	3238.5	-690.0	221	COM40	5385.8	686.0	301	SEG35	1555.2	680.0
62	VCHS	-2781.3	-690.0	142	LVSS	3314.7	-690.0	222	COM39	5334.0	686.0	302	SEG36	1512.0	680.0
63	VCHS	-2705.1	-690.0	143	LVSS	3390.9	-690.0	223	COM38	5282.2	686.0	303	SEG37	1468.8	680.0
64	VCHS	-2628.9	-690.0	144	LVSS	3467.1	-690.0	224	COM37	5230.4	686.0	304	SEG38	1425.6	680.0
65	VCC	-2552.7	-690.0	145	LVSS	3543.3	-690.0	225	COM36	5178.6	686.0	305	SEG39	1382.4	680.0
66	VCC	-2476.5	-690.0	146	NC	3619.5	-690.0	226	COM35	5126.8	686.0	306	SEG40	1339.2	680.0
67	VCOMH	-2400.3	-690.0	147	VCOMH	3695.7	-690.0	227	COM34	5075.0	686.0	307	SEG41	1296.0	680.0
68	VCOMH	-2324.1	-690.0	148	VCOMH	3771.9	-690.0	228	COM33	5023.2	686.0	308	SEG42	1252.8	680.0
69	VCOMH	-2247.9	-690.0	149	VCOMH	3848.1	-690.0	229	COM32	4971.4	686.0	309	SEG43	1209.6	680.0
70	VCOMH	-2171.7	-690.0	150	VCOMH	3924.3	-690.0	230	COM31	4919.6	686.0	310	SEG44	1166.4	680.0
71	VCOMH	-2095.5	-690.0	151	VCOMH	4000.5	-690.0	231	COM30	4867.8	686.0	311	SEG45	1123.2	680.0
72	VCOMH	-2019.3	-690.0	152	VCOMH	4076.7	-690.0	232	COM29	4816.0	686.0	312	SEG46	1080.0	680.0
73	VDD	-1943.1	-690.0	153	VDD	4152.9	-690.0	233	COM28	4764.2	686.0	313	SEG47	1036.8	680.0
74	VDD	-1866.9	-690.0	154	VDD	4229.1	-690.0	234	COM27	4712.4	686.0	314	SEG48	993.6	680.0
75	GPIO0	-1790.7	-690.0	155	VICON	4305.3	-690.0	235	COM26	4660.6	686.0	315	SEG49	950.4	680.0
76	GPIO1	-1714.5	-690.0	156	VICON	4381.5	-690.0	236	COM25	4608.8	686.0	316	SEG50	907.2	680.0
77	VSS	-1638.3	-690.0	157	VICON	4457.7	-690.0	237	COM24	4557.0	686.0	317	SEG51	864.0	680.0
78	VSS	-1562.1	-690.0	158	VICON	4533.9	-690.0	238	COM23	4505.2	686.0	318	SEG52	820.8	680.0
79	VSS	-1485.9	-690.0	159	VICON	4610.1	-690.0	239	COM22	4453.4	686.0	319	SEG53	777.6	680.0
80	LVSS	-1409.7	-690.0	160	VCC	4686.3	-690.0	240	COM21	4401.6	686.0	320	SEG54	734.4	680.0

Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis
321	SEG55	691.2	680.0	401	SEG120	-2764.8	680.0
322	SEG56	648.0	680.0	402	SEG121	-2808.0	680.0
323	SEG57	604.8	680.0	403	SEG122	-2851.2	680.0
324	SEG58	561.6	680.0	404	SEG123	-2894.4	680.0
325	SEG59	518.4	680.0	405	SEG124	-2937.6	680.0
326	DUMMY	475.2	680.0	406	SEG125	-2980.8	680.0
327	DUMMY	432.0	680.0	407	SEG126	-3024.0	680.0
328	DUMMY	388.8	680.0	408	SEG127	-3067.2	680.0
329	DUMMY	345.6	680.0	409	DUMMY	-3110.4	680.0
330	DUMMY	302.4	680.0	410	DUMMY	-3158.4	686.0
331	DUMMY	259.2	680.0	411	DUMMY	-3210.2	686.0
332	DUMMY	216.0	680.0	412	DUMMY	-3262.0	686.0
333	DUMMY	172.8	680.0	413	COM64	-3313.8	686.0
334	DUMMY	129.6	680.0	414	COM65	-3365.6	686.0
335	DUMMY	86.4	680.0	415	COM66	-3417.4	686.0
336	DUMMY	43.2	680.0	416	COM67	-3469.2	686.0
337	DUMMY	0.0	680.0	417	COM68	-3521.0	686.0
338	DUMMY	-43.2	680.0	418	COM69	-3572.8	686.0
339	DUMMY	-86.4	680.0	419	COM70	-3624.6	686.0
340	DUMMY	-129.6	680.0	420	COM71	-3676.4	686.0
341	SEG60	-172.8	680.0	421	COM72	-3728.2	686.0
342	SEG61	-216.0	680.0	422	COM73	-3780.0	686.0
343	SEG62	-259.2	680.0	423	COM74	-3831.8	686.0
344	SEG63	-302.4	680.0	424	COM75	-3883.6	686.0
345	SEG64	-345.6	680.0	425	COM76	-3935.4	686.0
346	SEG65	-388.8	680.0	426	COM77	-3987.2	686.0
347	SEG66	-432.0	680.0	427	COM78	-4039.0	686.0
348	SEG67	-475.2	680.0	428	COM79	-4090.8	686.0
349	SEG68	-518.4	680.0	429	COM80	-4142.6	686.0
350	SEG69	-561.6	680.0	430	COM81	-4194.4	686.0
351	SEG70	-604.8	680.0	431	COM82	-4246.2	686.0
352	SEG71	-648.0	680.0	432	COM83	-4298.0	686.0
353	SEG72	-691.2	680.0	433	COM84	-4349.8	686.0
354	SEG73	-734.4	680.0	434	COM85	-4401.6	686.0
355	SEG74	-777.6	680.0	435	COM86	-4453.4	686.0
356	SEG75	-820.8	680.0	436	COM87	-4505.2	686.0
357	SEG76	-864.0	680.0	437	COM88	-4557.0	686.0
358	SEG77	-907.2	680.0	438	COM89	-4608.8	686.0
359	SEG78	-950.4	680.0	439	COM90	-4660.6	686.0
360	SEG79	-993.6	680.0	440	COM91	-4712.4	686.0
361	SEG80	-1036.8	680.0	441	COM92	-4764.2	686.0
362	SEG81	-1080.0	680.0	442	COM93	-4816.0	686.0
363	SEG82	-1123.2	680.0	443	COM94	-4867.8	686.0
364	SEG83	-1166.4	680.0	444	COM95	-4919.6	686.0
365	SEG84	-1209.6	680.0	445	COM96	-4971.4	686.0
366	SEG85	-1252.8	680.0	446	COM97	-5023.2	686.0
367	SEG86	-1296.0	680.0	447	COM98	-5075.0	686.0
368	SEG87	-1339.2	680.0	448	COM99	-5126.8	686.0
369	SEG88	-1382.4	680.0	449	COM100	-5178.6	686.0
370	SEG89	-1425.6	680.0	450	COM101	-5230.4	686.0
371	SEG90	-1468.8	680.0	451	COM102	-5282.2	686.0
372	SEG91	-1512.0	680.0	452	COM103	-5334.0	686.0
373	SEG92	-1555.2	680.0	453	COM104	-5385.8	686.0
374	SEG93	-1598.4	680.0	454	COM105	-5437.6	686.0
375	SEG94	-1641.6	680.0	455	COM106	-5489.4	686.0
376	SEG95	-1684.8	680.0	456	COM107	-5541.2	686.0
377	SEG96	-1728.0	680.0	457	COM108	-5593.0	686.0
378	SEG97	-1771.2	680.0	458	COM109	-5644.8	686.0
379	SEG98	-1814.4	680.0	459	COM110	-5696.6	686.0
380	SEG99	-1857.6	680.0	460	COM111	-5748.4	686.0
381	SEG100	-1900.8	680.0	461	COM112	-5800.2	686.0
382	SEG101	-1944.0	680.0	462	COM113	-5852.0	686.0
383	SEG102	-1987.2	680.0	463	COM114	-5903.8	686.0
384	SEG103	-2030.4	680.0	464	COM115	-5955.6	686.0
385	SEG104	-2073.6	680.0	465	COM116	-6007.4	686.0
386	SEG105	-2116.8	680.0	466	COM117	-6059.2	686.0
387	SEG106	-2160.0	680.0	467	COM118	-6111.0	686.0
388	SEG107	-2203.2	680.0	468	COM119	-6162.8	686.0
389	SEG108	-2246.4	680.0	469	COM120	-6214.6	686.0
390	SEG109	-2289.6	680.0	470	COM121	-6266.4	686.0
391	SEG110	-2332.8	680.0	471	COM122	-6318.2	686.0
392	SEG111	-2376.0	680.0	472	COM123	-6370.0	686.0
393	SEG112	-2419.2	680.0	473	COM124	-6421.8	686.0
394	SEG113	-2462.4	680.0	474	COM125	-6473.6	686.0
395	SEG114	-2505.6	680.0	475	COM126	-6525.4	686.0
396	SEG115	-2548.8	680.0	476	COM127	-6577.2	686.0
397	SEG116	-2592.0	680.0	477	DUMMY	-6640.0	686.0
398	SEG117	-2635.2	680.0				
399	SEG118	-2678.4	680.0				
400	SEG119	-2721.6	680.0				

6 PIN ARRANGEMENT

6.1 SSD1329UR1 pin assignment

Figure 6-1 : SSD1329UR1 Pin Assignment

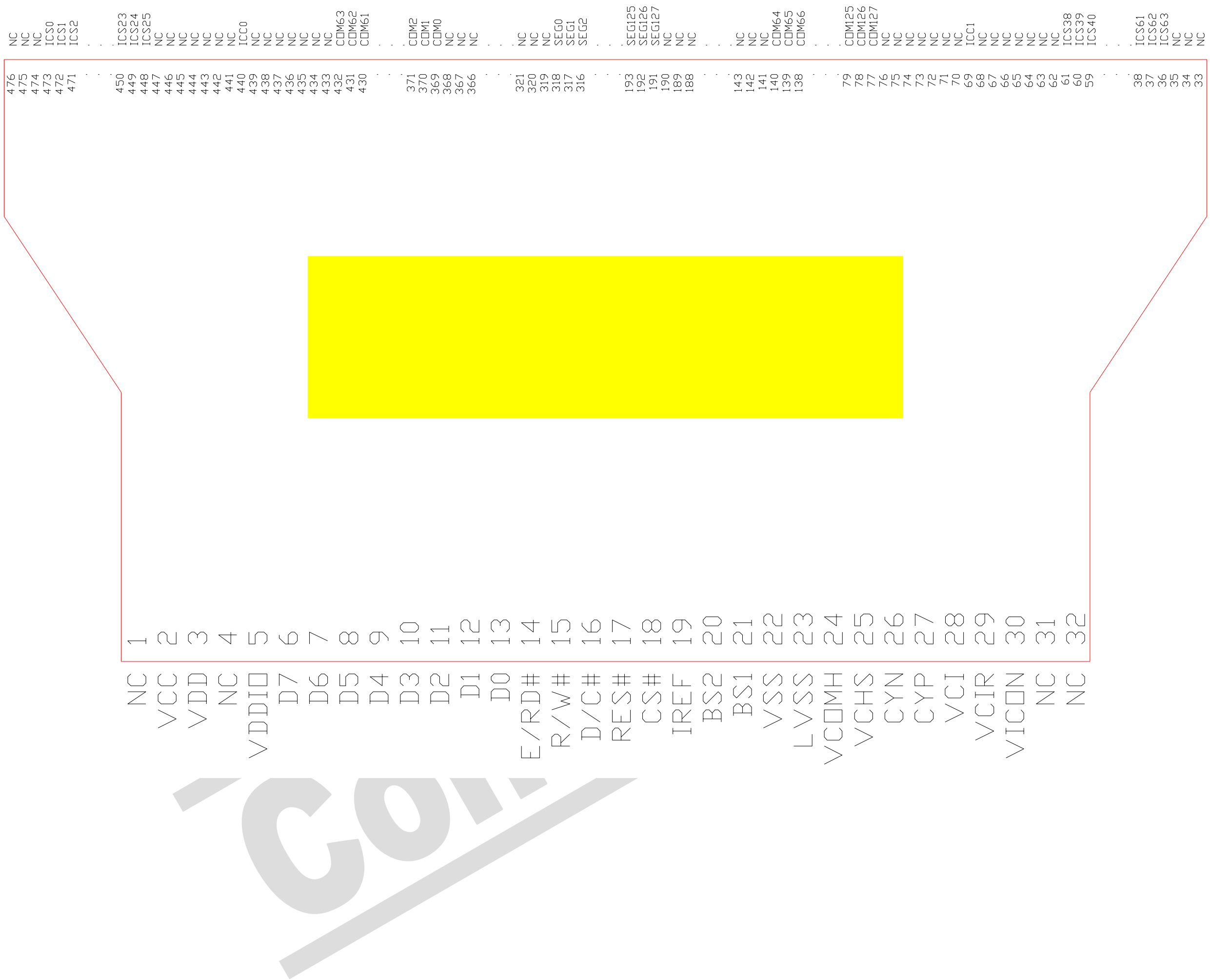


Table 6-1 : SSD1329UR1 Pin Assignment Table

Pad #	Pad Name	Pad #	Pad Name	Pad #	Pad Name	Pad #	Pad Name	Pad #	Pad Name	Pad #	Pad Name
1	NC	81	COM123	161	NC	241	SEG77	321	NC	401	COM32
2	VCC	82	COM122	162	NC	242	SEG76	322	NC	402	COM33
3	VDD	83	COM121	163	NC	243	SEG75	323	NC	403	COM34
4	NC	84	COM120	164	NC	244	SEG74	324	NC	404	COM35
5	VDDIO	85	COM119	165	NC	245	SEG73	325	NC	405	COM36
6	D7	86	COM118	166	NC	246	SEG72	326	NC	406	COM37
7	D6	87	COM117	167	NC	247	SEG71	327	NC	407	COM38
8	D5	88	COM116	168	NC	248	SEG70	328	NC	408	COM39
9	D4	89	COM115	169	NC	249	SEG69	329	NC	409	COM40
10	D3	90	COM114	170	NC	250	SEG68	330	NC	410	COM41
11	D2	91	COM113	171	NC	251	SEG67	331	NC	411	COM42
12	D1	92	COM112	172	NC	252	SEG66	332	NC	412	COM43
13	D0	93	COM111	173	NC	253	SEG65	333	NC	413	COM44
14	E/RD#	94	COM110	174	NC	254	SEG64	334	NC	414	COM45
15	R/W#	95	COM109	175	NC	255	SEG63	335	NC	415	COM46
16	D/C#	96	COM108	176	NC	256	SEG62	336	NC	416	COM47
17	RES#	97	COM107	177	NC	257	SEG61	337	NC	417	COM48
18	CS#	98	COM106	178	NC	258	SEG60	338	NC	418	COM49
19	IREF	99	COM105	179	NC	259	SEG59	339	NC	419	COM50
20	BS2	100	COM104	180	NC	260	SEG58	340	NC	420	COM51
21	BS1	101	COM103	181	NC	261	SEG57	341	NC	421	COM52
22	VSS	102	COM102	182	NC	262	SEG56	342	NC	422	COM53
23	LVSS	103	COM101	183	NC	263	SEG55	343	NC	423	COM54
24	VCOMH	104	COM100	184	NC	264	SEG54	344	NC	424	COM55
25	VCHS	105	COM99	185	NC	265	SEG53	345	NC	425	COM56
26	CYN	106	COM98	186	NC	266	SEG52	346	NC	426	COM57
27	CYP	107	COM97	187	NC	267	SEG51	347	NC	427	COM58
28	VCI1	108	COM96	188	NC	268	SEG50	348	NC	428	COM59
29	VCIR	109	COM95	189	NC	269	SEG49	349	NC	429	COM60
30	VICON	110	COM94	190	NC	270	SEG48	350	NC	430	COM61
31	NC	111	COM93	191	SEG127	271	SEG47	351	NC	431	COM62
32	NC	112	COM92	192	SEG126	272	SEG46	352	NC	432	COM63
33	NC	113	COM91	193	SEG125	273	SEG45	353	NC	433	NC
34	NC	114	COM90	194	SEG124	274	SEG44	354	NC	434	NC
35	NC	115	COM89	195	SEG123	275	SEG43	355	NC	435	NC
36	ICS63	116	COM88	196	SEG122	276	SEG42	356	NC	436	NC
37	ICS62	117	COM87	197	SEG121	277	SEG41	357	NC	437	NC
38	ICS61	118	COM86	198	SEG120	278	SEG40	358	NC	438	NC
39	ICS60	119	COM85	199	SEG119	279	SEG39	359	NC	439	NC
40	ICS59	120	COM84	200	SEG118	280	SEG38	360	NC	440	ICC0
41	ICS58	121	COM83	201	SEG117	281	SEG37	361	NC	441	NC
42	ICS57	122	COM82	202	SEG116	282	SEG36	362	NC	442	NC
43	ICS56	123	COM81	203	SEG115	283	SEG35	363	NC	443	NC
44	ICS55	124	COM80	204	SEG114	284	SEG34	364	NC	444	NC
45	ICS54	125	COM79	205	SEG113	285	SEG33	365	NC	445	NC
46	ICS53	126	COM78	206	SEG112	286	SEG32	366	NC	446	NC
47	ICS52	127	COM77	207	SEG111	287	SEG31	367	NC	447	NC
48	ICS51	128	COM76	208	SEG110	288	SEG30	368	NC	448	ICS25
49	ICS50	129	COM75	209	SEG109	289	SEG29	369	COM0	449	ICS24
50	ICS49	130	COM74	210	SEG108	290	SEG28	370	COM1	450	ICS23
51	ICS48	131	COM73	211	SEG107	291	SEG27	371	COM2	451	ICS22
52	ICS47	132	COM72	212	SEG106	292	SEG26	372	COM3	452	ICS21
53	ICS46	133	COM71	213	SEG105	293	SEG25	373	COM4	453	ICS20
54	ICS45	134	COM70	214	SEG104	294	SEG24	374	COM5	454	ICS19
55	ICS44	135	COM69	215	SEG103	295	SEG23	375	COM6	455	ICS18
56	ICS43	136	COM68	216	SEG102	296	SEG22	376	COM7	456	ICS17
57	ICS42	137	COM67	217	SEG101	297	SEG21	377	COM8	457	ICS16
58	ICS41	138	COM66	218	SEG100	298	SEG20	378	COM9	458	ICS15
59	ICS40	139	COM65	219	SEG99	299	SEG19	379	COM10	459	ICS14
60	ICS39	140	COM64	220	SEG98	300	SEG18	380	COM11	460	ICS13
61	ICS38	141	NC	221	SEG97	301	SEG17	381	COM12	461	ICS12
62	NC	142	NC	222	SEG96	302	SEG16	382	COM13	462	ICS11
63	NC	143	NC	223	SEG95	303	SEG15	383	COM14	463	ICS10
64	NC	144	NC	224	SEG94	304	SEG14	384	COM15	464	ICS9
65	NC	145	NC	225	SEG93	305	SEG13	385	COM16	465	ICS8
66	NC	146	NC	226	SEG92	306	SEG12	386	COM17	466	ICS7
67	NC	147	NC	227	SEG91	307	SEG11	387	COM18	467	ICS6
68	NC	148	NC	228	SEG90	308	SEG10	388	COM19	468	ICS5
69	ICC1	149	NC	229	SEG89	309	SEG9	389	COM20	469	ICS4
70	NC	150	NC	230	SEG88	310	SEG8	390	COM21	470	ICS3
71	NC	151	NC	231	SEG87	311	SEG7	391	COM22	471	ICS2
72	NC	152	NC	232	SEG86	312	SEG6	392	COM23	472	ICS1
73	NC	153	NC	233	SEG85	313	SEG5	393	COM24	473	ICS0
74	NC	154	NC	234	SEG84	314	SEG4	394	COM25	474	NC
75	NC	155	NC	235	SEG83	315	SEG3	395	COM26	475	NC
76	NC	156	NC	236	SEG82	316	SEG2	396	COM27	476	NC
77	COM127	157	NC	237	SEG81	317	SEG1	397	COM28		
78	COM126	158	NC	238	SEG80	318	SEG0	398	COM29		
79	COM125	159	NC	239	SEG79	319	NC	399	COM30		
80	COM124	160	NC	240	SEG78	320	NC	400	COM31		

6.2 SSD1329U1 pin assignment

Figure 6-2 : SSD1329U1 Pin Assignment

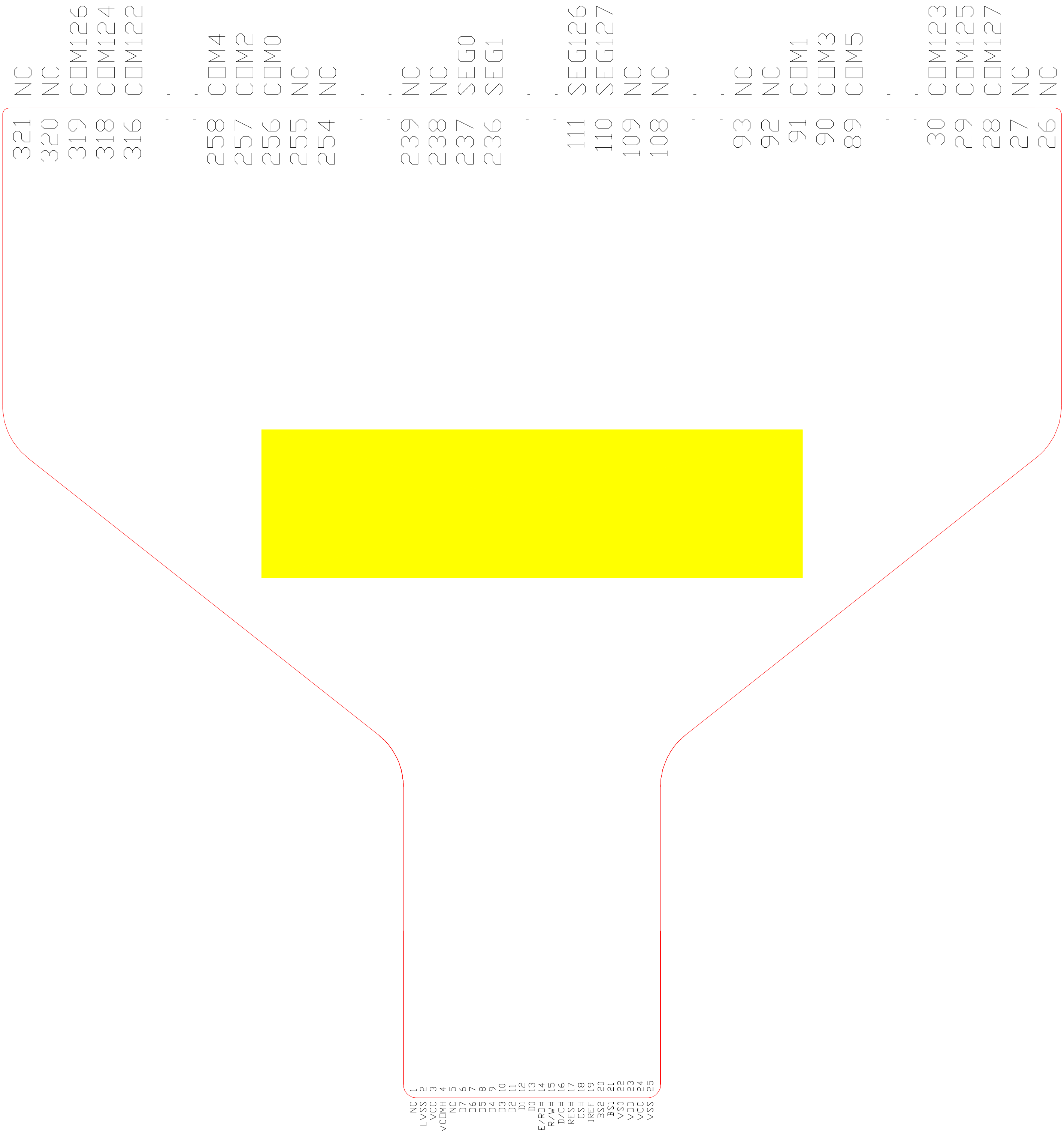


Table 6-1 : SSD1329U1 Pin Assignment Table

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NC	81	COM21	161	SEG76	241	NC	321	NC
2	LVSS	82	COM19	162	SEG75	242	NC		
3	VCC	83	COM17	163	SEG74	243	NC		
4	VCOMH	84	COM15	164	SEG73	244	NC		
5	NC	85	COM13	165	SEG72	245	NC		
6	D7	86	COM11	166	SEG71	246	NC		
7	D6	87	COM9	167	SEG70	247	NC		
8	D5	88	COM7	168	SEG69	248	NC		
9	D4	89	COM5	169	SEG68	249	NC		
10	D3	90	COM3	170	SEG67	250	NC		
11	D2	91	COM1	171	SEG66	251	NC		
12	D1	92	NC	172	SEG65	252	NC		
13	D0	93	NC	173	SEG64	253	NC		
14	RD	94	NC	174	SEG63	254	NC		
15	R/W	95	NC	175	SEG62	255	NC		
16	D/C	96	NC	176	SEG61	256	COM0		
17	RES	97	NC	177	SEG60	257	COM2		
18	CS	98	NC	178	SEG59	258	COM4		
19	IREF	99	NC	179	SEG58	259	COM6		
20	BS2	100	NC	180	SEG57	260	COM8		
21	BS1	101	NC	181	SEG56	261	COM10		
22	BS0	102	NC	182	SEG55	262	COM12		
23	VDD	103	NC	183	SEG54	263	COM14		
24	VCC	104	NC	184	SEG53	264	COM16		
25	VSS	105	NC	185	SEG52	265	COM18		
26	NC	106	NC	186	SEG51	266	COM20		
27	NC	107	NC	187	SEG50	267	COM22		
28	COM127	108	NC	188	SEG49	268	COM24		
29	COM125	109	NC	189	SEG48	269	COM26		
30	COM123	110	SEG127	190	SEG47	270	COM28		
31	COM121	111	SEG126	191	SEG46	271	COM30		
32	COM119	112	SEG125	192	SEG45	272	COM32		
33	COM117	113	SEG124	193	SEG44	273	COM34		
34	COM115	114	SEG123	194	SEG43	274	COM36		
35	COM113	115	SEG122	195	SEG42	275	COM38		
36	COM111	116	SEG121	196	SEG41	276	COM40		
37	COM109	117	SEG120	197	SEG40	277	COM42		
38	COM107	118	SEG119	198	SEG39	278	COM44		
39	COM105	119	SEG118	199	SEG38	279	COM46		
40	COM103	120	SEG117	200	SEG37	280	COM48		
41	COM101	121	SEG116	201	SEG36	281	COM50		
42	COM99	122	SEG115	202	SEG35	282	COM52		
43	COM97	123	SEG114	203	SEG34	283	COM54		
44	COM95	124	SEG113	204	SEG33	284	COM56		
45	COM93	125	SEG112	205	SEG32	285	COM58		
46	COM91	126	SEG111	206	SEG31	286	COM60		
47	COM89	127	SEG110	207	SEG30	287	COM62		
48	COM87	128	SEG109	208	SEG29	288	COM64		
49	COM85	129	SEG108	209	SEG28	289	COM66		
50	COM83	130	SEG107	210	SEG27	290	COM68		
51	COM81	131	SEG106	211	SEG26	291	COM70		
52	COM79	132	SEG105	212	SEG25	292	COM72		
53	COM77	133	SEG104	213	SEG24	293	COM74		
54	COM75	134	SEG103	214	SEG23	294	COM76		
55	COM73	135	SEG102	215	SEG22	295	COM78		
56	COM71	136	SEG101	216	SEG21	296	COM80		
57	COM69	137	SEG100	217	SEG20	297	COM82		
58	COM67	138	SEG99	218	SEG19	298	COM84		
59	COM65	139	SEG98	219	SEG18	299	COM86		
60	COM63	140	SEG97	220	SEG17	300	COM88		
61	COM61	141	SEG96	221	SEG16	301	COM90		
62	COM59	142	SEG95	222	SEG15	302	COM92		
63	COM57	143	SEG94	223	SEG14	303	COM94		
64	COM55	144	SEG93	224	SEG13	304	COM96		
65	COM53	145	SEG92	225	SEG12	305	COM98		
66	COM51	146	SEG91	226	SEG11	306	COM100		
67	COM49	147	SEG90	227	SEG10	307	COM102		
68	COM47	148	SEG89	228	SEG9	308	COM104		
69	COM45	149	SEG88	229	SEG8	309	COM106		
70	COM43	150	SEG87	230	SEG7	310	COM108		
71	COM41	151	SEG86	231	SEG6	311	COM110		
72	COM39	152	SEG85	232	SEG5	312	COM112		
73	COM37	153	SEG84	233	SEG4	313	COM114		
74	COM35	154	SEG83	234	SEG3	314	COM116		
75	COM33	155	SEG82	235	SEG2	315	COM118		
76	COM31	156	SEG81	236	SEG1	316	COM120		
77	COM29	157	SEG80	237	SEG0	317	COM122		
78	COM27	158	SEG79	238	NC	318	COM124		
79	COM25	159	SEG78	239	NC	319	COM126		
80	COM23	160	SEG77	240	NC	320	NC		

7 PIN DESCRIPTIONS

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin

Table 7-1 : Pin Descriptions

Pin Name	Pin Type	Description
RES#	I	This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin high during normal operation.
CS#	I	This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
D/C#	I	This pin is Data/Command control pin. When the pin is pulled high, the data at D_7-D_0 is treated as data. When the pin is pulled low, the data at D_7-D_0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams in Figure 13-1, Figure 13-2, Figure 13-3.
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.
R/W# (WR#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled high and write mode will be carried out when low. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected.
D_7-D_0	IO	These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.
BS[2:0]	I	MCU bus interface selection pins. Please refer to Table 7-2 for the details of the selection.
V_{DDIO}	P	This pin is a power supply pin of I/O buffer. It should be connected to V_{DD} or external source. All I/O signal should have voltage high reference to V_{DDIO}. When I/O signal pins (BS0, BS1, BS2, CLS, CL, D0-D7, interface signals…) pull high, they should be connected to V_{DDIO}.
V_{DD}	P	Power Supply pin. It must be connected to external source.
V_{SS}, LV_{SS}	P	These pins are ground pin and also act as ground reference for the logic pins. They must be connected to external ground.
CL	I	This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. When internal oscillator is disabled, this pin receives display clock signal from external clock source.
CLS	I	This pin is internal clock enable. When this pin is pulled high, internal oscillator is selected. The internal clock will be disabled when it is pulled low, an external clock source must be connected to CL pin for normal operation.
V_{CC}	P	This is the most positive voltage supply pin of the chip. It is supplied either by external high voltage source or internal booster.

Pin Name	Pin Type	Description
V_{COMH}	IO	This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When V_{COMH} is generated internally, a capacitor should be connected between this pin and V_{SS}.
I_{REF}	IO	This pin is the segment output current reference pin. I_{SEG} is derived from I_{REF}. A resistor should be connected between this pin and V_{DD} to maintain the current around 10uA.
COM0 ~ COM127	O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off.
SEG0 ~ SEG127	O	These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off.
ICS0 ~ ICS63	O	These pins provide the Segment driving signals for hard icons.
ICC0 ~ ICC1	O	These pins provide the Common driving signals for hard icons.
VCI	P	This is the power supply pin of hard icon DC-DC voltage converter. It must be supplied externally.
VICON	P	This is the power output pin for DC-DC converter to drive hard icons. A 2uF capacitor is recommended to connect from this pin to the ground. If internal DC-DC converter is disabled, this pin is acted as the power input pin for hard icons.
VCHS	P	This is the ground pin for hard icons DC-DC voltage converter. It must be connected to external ground.
CYP, CYN	O	These pins are used to connect a capacitor between the PMOS and NMOS for hard icons DC-DC voltage converter. The recommended value of this capacitor is 1uF.
VCIR	O	This pin is used to connect a resistor between VCI and it when internal charge pump is used. The recommended value of this resistor is 20Ω.

Table 7-2 : MCU Bus Interface Pin Selection

Pin Name	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS0	0	0	0
BS1	0	1	0
BS2	1	1	0

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MPU Interface selection

8.1.1 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/W, D/C#, E and CS#.

A low in R/W indicates WRITE operation and high in R/W indicates READ operation.
A low in D/C indicates COMMAND read/write and high in D/C indicates DATA read/write.
The E input serves as data latch signal while CS# is low. Data is latched at the falling edge of E signal.

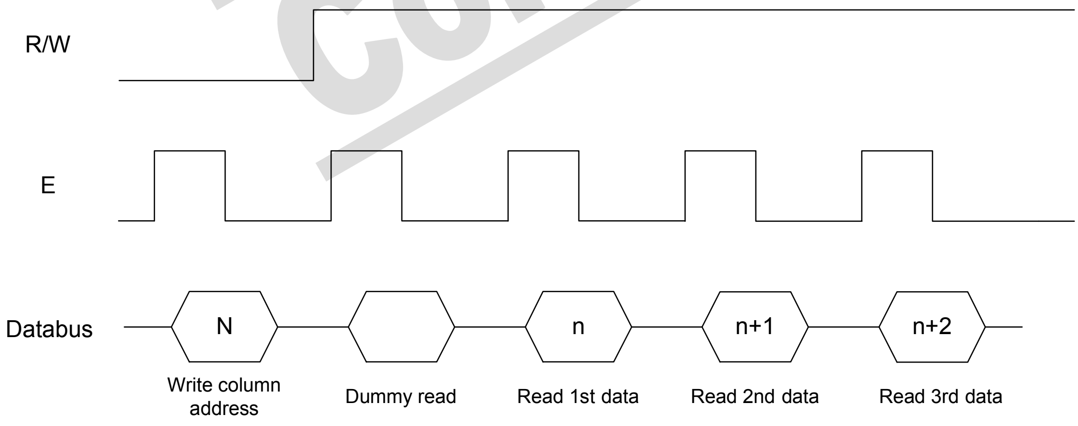
Table 8-1 : Control pins of 6800 interface

Function	**E**	**R/W**	**CS#**	**D/C#**
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1)↓ stands for falling edge of signal
H stands for high in signal
L stands for low in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), RD#, WR#, D/C# and CS#.

A low in D/C# indicates COMMAND read/write and high in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept low.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept low.

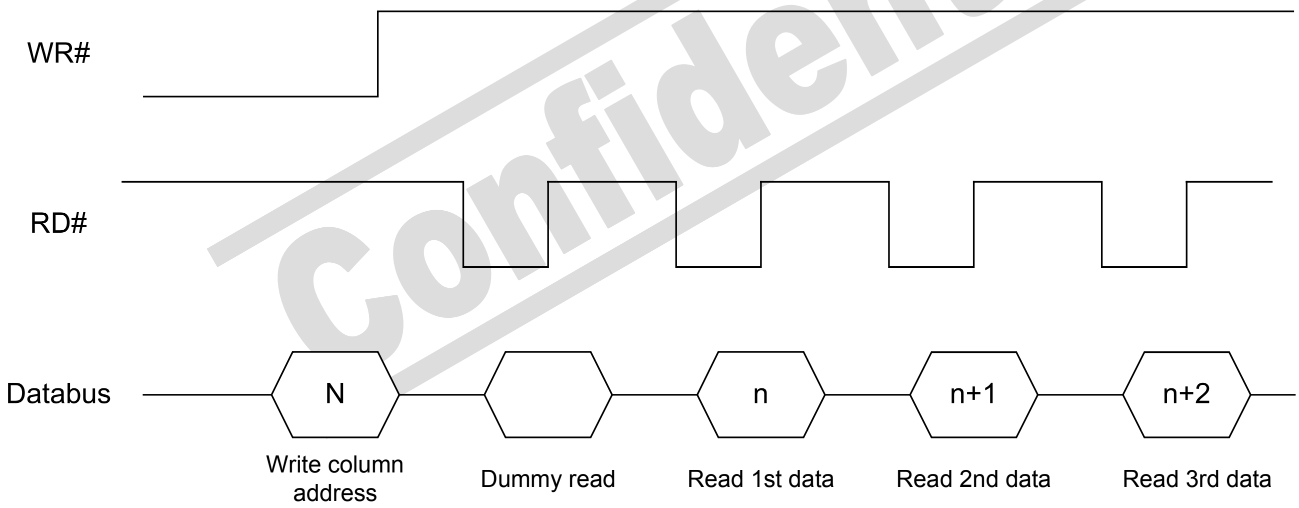
Table 8-2 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
H stands for high in signal
L stands for low in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-2.

Figure 8-2 : Display data read back procedure - insertion of dummy read



Alternatively, RD# and WR# can be keep stable while CS# is serve as the data/command latch signal.

Table 8-3 : Control pins of 8080 interface (Alternative form)

Function	RD#	WR#	CS#	D/C
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note
(1) ↑ stands for rising edge of signal
H stands for high in signal
L stands for low in signal

8.1.3 MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W can be connected to an external ground.

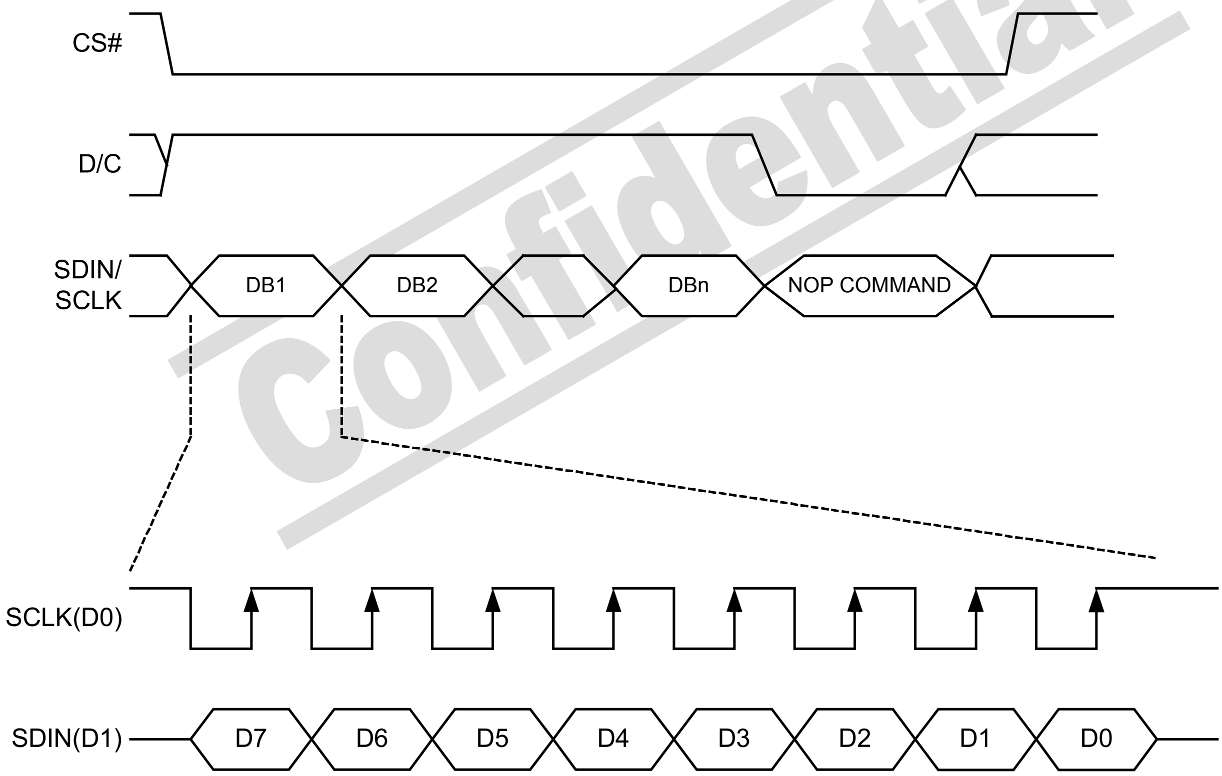
Table 8-4 : Control pins of Serial interface

Function	E	R/W	CS#	D/C
Write command	Tie low	Tie low	L	L
Write data	Tie low	Tie low	L	H

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D_7, D_6, ... D_0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed. And during data writing, an additional NOP command should be inserted before the CS# goes high as shown in Figure 8-3

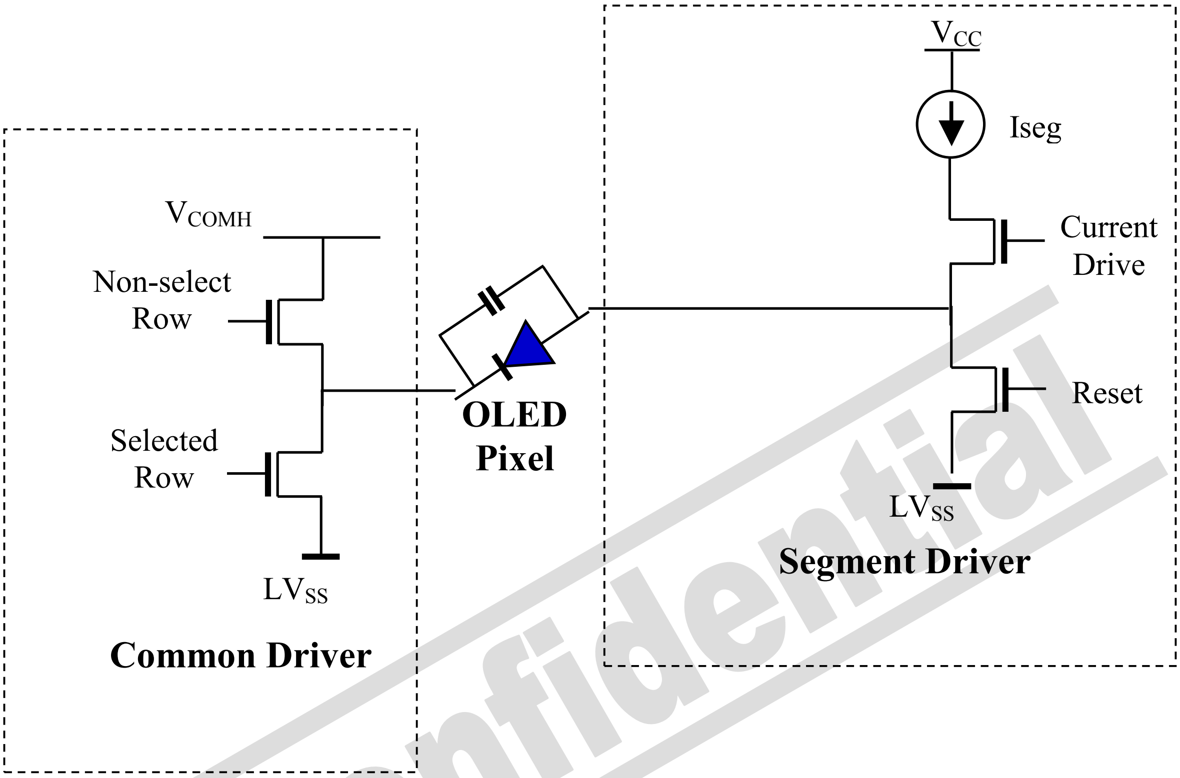
Figure 8-3 : Display data write procedure in SPI mode



8.2 Segment Drivers/Common Drivers

Segment drivers have 128 current sources to drive OLED panel. The driving current can be adjusted from 0 to 300uA with 8 bits, 256 steps. Common drivers generate voltage scanning pulses. The block diagrams and waveforms of the segment and common driver are shown as follow.

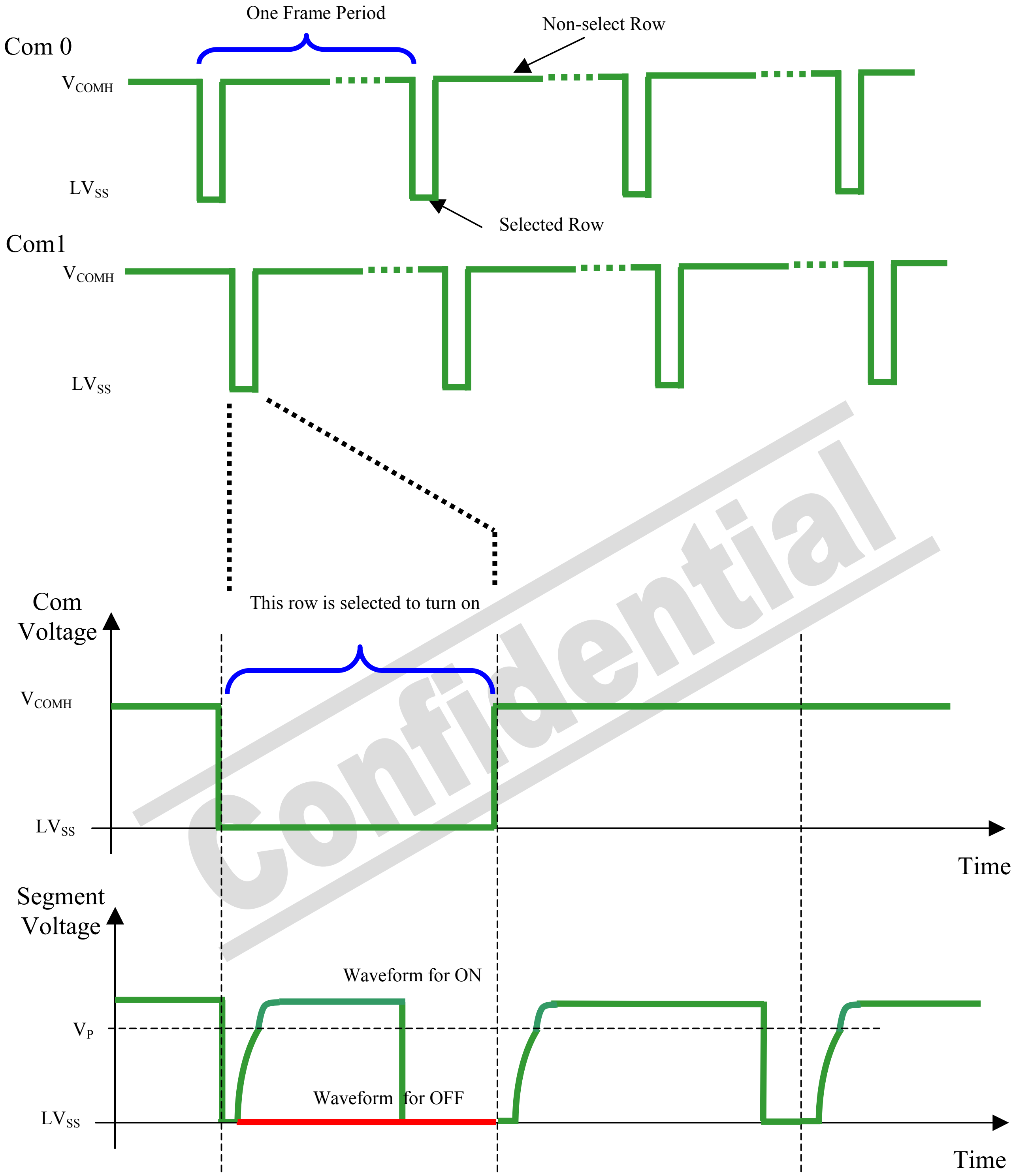
Figure 8-4 : Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 8-5.

In the scanned row, the pixels on the row will be turned on or off by sending the corresponding data signal to the segment pins. If the pixel is turned off, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned on.

Figure 8-5 : Segment and Common Driver Signal Waveform



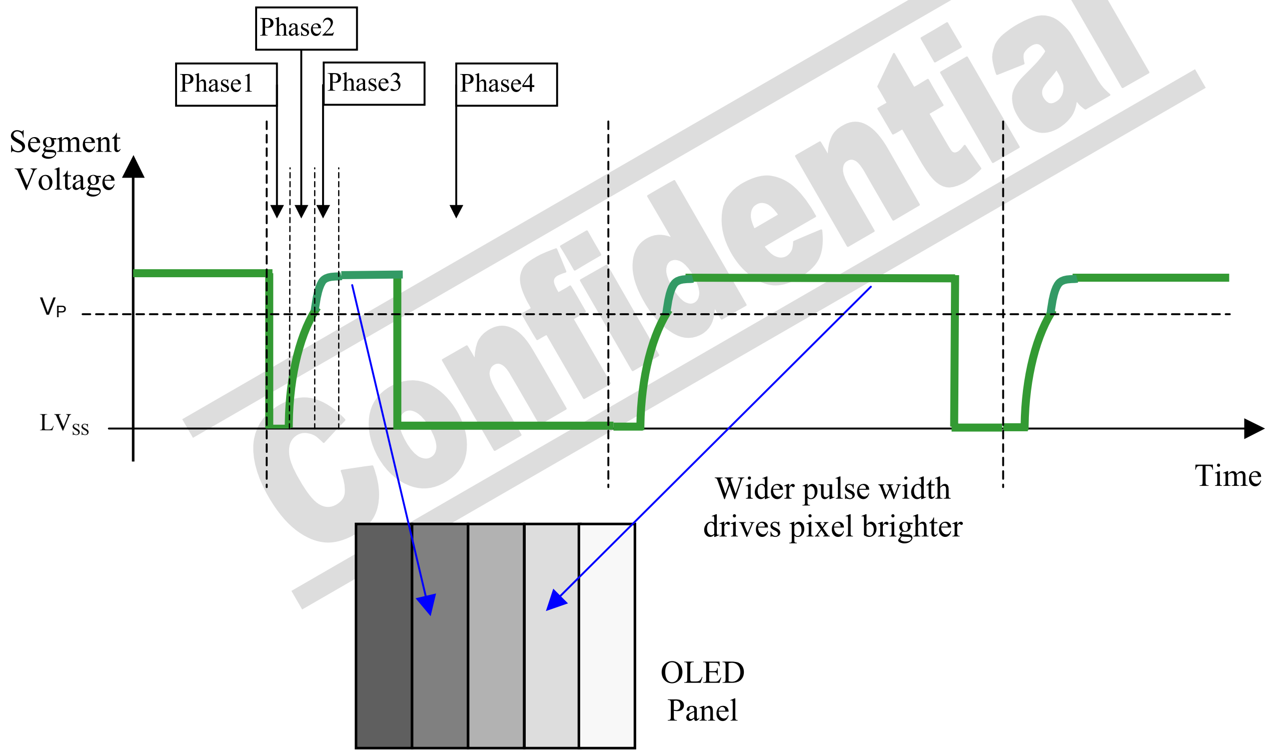
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to LV_{SS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0] from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, voltage pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from LV_{SS}. The amplitude of V_P can be programmed by the command BCh. The period of phase 2 can be programmed in length from 1 to 16 DCLK by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted current through current pre-charge. The current pre-charge can speed up the charging process. The period of phase 3 can be programmed by command BBh.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The wider pulse widths in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.

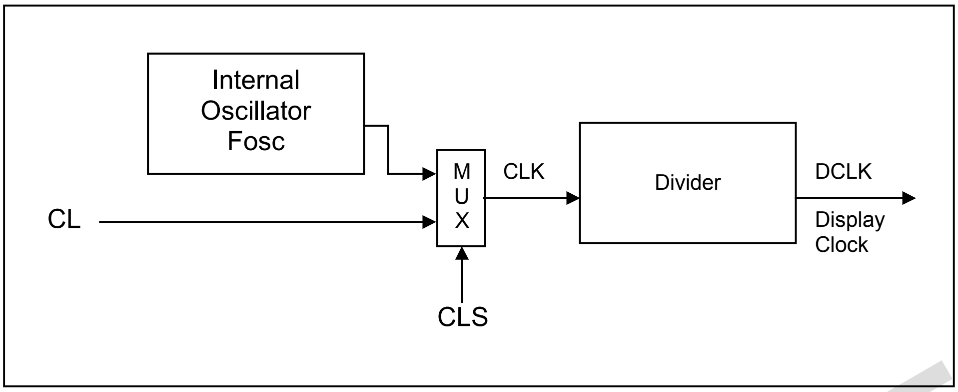
Figure 8-6: Gray Scale Control by PWM in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.
The length of phase 4 is defined by command B7h “Set Default Gray Scale Table” or B8h “Set Gray Scale Table”. In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

8.3 Oscillator Circuit and Display Time Generator

Figure 8-7 : Oscillator Circuit and Display Time Generator



This module is an On-Chip low power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled high, internal oscillator is chosen and CL should be left open. Pulling CLS pin low disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command B3h, please refer to Table 9-1.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command B3h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16.
- K is row period. It is configured by command B2h. This value should comply with following condition.
  $$K \geq \text{Phase 1} + \text{Phase 2} + \text{Phase 3} + \text{GS15}$$
- Number of multiplex ratio is set by command A8h. The power on reset value is 7Fh.
- F_{OSC} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in faster frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.4 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is high, D_7-D_0 is treated as either the data bytes of multiple byte command or display data written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D_7-D_0 is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

8.5 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 128 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80H

8.6 Current Control and Voltage Control

This block is used to derive the incoming power sources into the different levels of internal use voltage and current. V_{CC} and V_{DD} are external power supplies. I_{REF} is a reference current source for segment current drivers.

8.7 Hard icons column and row drivers

There are 64 segment drivers as the current sources to hard icons and 2 common drivers with 2 pins each to sink the current. The hard icons drivers support either DC or AC driving method.

8.8 DC-DC converter for Hard icons

It is a 2X charge-pump type voltage generator circuit. It doubles the voltage input VCI to generate VICON. VICON is the voltage supply to the hard icons driver.

8.9 Gray Scale Decoder

In SSD1329 there are 16 gray levels from GS0 to GS15. The gray scale of the display is defined by the pulse width (PW) of current drive phase, except GS0 there is no pre-charge (phase 2,3) and current drive (phase 4).

8.10 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps in Table 8-5 to Table 8-9 show some examples on using the command "Set Re-map" A0h to re-map the GDDRAM. In the following tables, the lower nipple and higher nibble of D0 ,D1, D2, …,D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

Table 8-5 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to :
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

Table 8-5 : GDDRAM Address Map 1

COM Outputs	Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address (HEX)
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|					|					
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]	
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]	

Nibble Re-map A[1]=0

Table 8-6 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to :
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Vertical Address Increment (A[2]=1)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

Table 8-6 : GDDRAM Address Map 2

COM Outputs	Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address (HEX)
COM0	00	D0[3:0]	D0[7:4]	D128[3:0]	D128[7:4]		D7936[3:0]	D7936[7:4]	D8064[3:0]	D8064[7:4]	
COM1	01	D1[3:0]	D1[7:4]	D129[3:0]	D129[7:4]		D7937[3:0]	D7937[7:4]	D8065[3:0]	D8065[7:4]	
|	|					|					
COM126	7E	D126[3:0]	D126[7:4]	D254[3:0]	D254[7:4]		D8062[3:0]	D8062[7:4]	D8190[3:0]	D8190[7:4]	
COM127	7F	D127[3:0]	D127[7:4]	D255[3:0]	D255[7:4]		D8063[3:0]	D8063[7:4]	D8191[3:0]	D8191[7:4]	

(Display Startline=0)

Nibble Re-map A[1]=0

Table 8-7 shows the GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to :
  - Enable Column Address Re-map (A[0]=1)
  - Enable Nibble Re-map (A[1]=1)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D8191

Table 8-7 : GDDRAM Address Map 3

COM Outputs (Display Startline=0)	Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		3F		3E			01		00		Column Address (HEX)
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
|	|					|					
COM126	7E	D8127[7:4]	D8127[3:0]	D8126[7:4]	D8126[3:0]		D8065[7:4]	D8065[3:0]	D8064[7:4]	D8064[3:0]	
COM127	7F	D8191[7:4]	D8191[3:0]	D8190[7:4]	D8190[3:0]		D8129[7:4]	D8129[3:0]	D8128[7:4]	D8128[3:0]	

Nibble Re-map A[1]=1

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display. The Table 8-8 shows the example in which the display start line register is set to 78H with the following condition:

- Command “Set Re-map” A0h is set to :
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 … D8191

Table 8-8 : GDDRAM Address Map 4

COM Outputs (Display Startline=78H)	Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address (HEX)
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM118	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
|	|					|					
COM121	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]	
COM120	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]	

Nibble Re-map A[1]=0

Table 8-9 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to :
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 … D7811

Table 8-9 : GDDRAM Address Map 5

COM Outputs (Display Startline=0)	Row Address (HEX)	SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
	Column Address (HEX)	00		01			3E		3F	
COM0	00									
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]		
|	|									
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]		
COM127	7F									

SEG Outputs
Column Address (HEX)

Nibble Re-map A[1]=0

Note

(1) Please refer to Table 9-1 for the details of setting command "Set Re-map"A0h.
(2) The "Display Start Line" is set by the command "Set Display Start Line" A1h and please refer to Table for the setting details
(3) The "Column Start/End Address" is set by the command "Set Column Address" 15h and please refer to Table 9-1 for the setting details
(4) The "Row Start/End Address" is set by the command "Set Row Address" 75h and please refer to Table 9-1 for the setting details

9 COMMAND TABLE

Table 9-1 : Command Table

(D/C# = 0, R/W# (WR#) = 0, E(RD#) = 1) unless specific setting is stated

Fundamental Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 0 0	15 A[5:0] B[5:0]	0 * *	0 * *	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup Column start and end address A[5:0]: Start Address, range:00h-3Fh, [RESET = 00h] B[5:0]: End Address, range:00h-3Fh, [RESET = 3Fh]
0 0 0	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	Setup Row start and end address A[6:0]: Start Address, range:00h-7Fh, [RESET = 00h] B[6:0]: End Address, range:00h-7Fh, [RESET = 7Fh]
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Current	A[7:0]: Contrast Value, range:0~ 255, [RESET = 80h]
0 0	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Pre-charge Current	A[7:1]: Set Pre-charge Current A[7:1] = 00h, Pre-charge current = 1uA A[7:1] = 01h, Pre-charge current = 3uA : A[7:1] = 7Fh, Pre-charge current = 255uA The RESET value of A[7:1] depends on the value of the contrast current (81h) and is equal to: 2*81h A[7:0] +1 (maximum 7Fh) A[0] = 0, Disable double the Pre-charge current (RESET) A[0] = 1, Enable double the Pre-charge current **Note** (1) The final output current should be < 500 uA.
0 0	90 A[7:0]	1 *	0 *	0 A_5	1 A_4	0 *	0 *	0 A_1	0 A_0	Set Master Icon Control	A[7:0]: Icon control [RESET = 00h] A[1:0] = 00b, Icon RESET to normal display (RESET) A[1:0] = 01b, Icon All ON (without altering icon ON / OFF register) A[1:0] = 10b, Icon All OFF (without altering icon ON/ OFF register) A[4] = 0, Disable icon display (RESET) A[4] = 1, Enable icon display A[5] = 0, Disable VICON charge pump circuit (RESET) A[5] = 1, Enable VICON charge pump circuit

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 0	91 A[7:0]	1 A_7	0 A_6	0 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Icon Current Range	A[6:0]: Icon current [RESET = 7Fh] A[7:0] = 00h, max icon current = 0.0uA A[7:0] = 01h, max icon current = 0.5uA A[7:0] = 02h, max icon current = 1.0uA A[7:0] = 03h, max icon current = 1.5uA A[7:0] = 04h, max icon current = 2.0uA … … … A[7:0] = FCh, max icon current = 126.0uA A[7:0] = FDh, max icon current = 126.5uA A[7:0] = FEh, max icon current = 127.0uA A[7:0] = FFh, max icon current = 127.5uA (RESET) **Note** (1) The larger the icon current range, the better the uniformity
0 0 0 … … 0 0	92 A0[6:0] A1[6:0] … … A62[6:0] A63[6:0]	1 * * ... ... * *	0 $A0_6$ $A1_6$ ... ... $A62_6$ $A63_6$	0 $A0_5$ $A1_5$ ... ... $A62_5$ $A63_5$	1 $A0_4$ $A1_4$ ... ... $A62_4$ $A63_4$	0 $A0_3$ $A1_3$ ... ... $A62_3$ $A63_3$	0 $A0_2$ $A1_2$ ... ... $A62_2$ $A63_2$	1 $A0_1$ $A1_1$ ... ... $A62_1$ $A63_1$	0 $A0_0$ $A1_0$ ... ... $A62_0$ $A63_0$	Set Individual Icon Current	Each Icon Current is set by the formula: (A[6:0] / 127) x max icon current, where the max icon current is defined by the command "Set icon current range" 91h. e.g. Icon Current of ICS0 = (A0[6:0]/127) x max icon current. A0[6:0] : icon current for ICS0, range: 00h-7Fh A1[6:0] : icon current for ICS1, range: 00h-7Fh … … … A63[6:0] : icon current for ICS62, range: 00h-7Fh A64[6:0] : icon current for ICS63, range: 00h-7Fh **Note** (1) All 64 levels (1 level for each ICS signals) of icon current must be entered to operate this command properly. (2) The icon current of the unselected icon pins must be set to zero by this command.
0 0	93 A[7:0]	1 A_7	0 A_6	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Individual Icon ON / OFF Register	Individual icon selection: A[5:0]: select one of the 64 icons from ICS0 ~ ICS63 A[7:6] = 00b, turn OFF selected icon A[7:6] = 01b, turn ON selected icon A[7:6] = 11b, blink selected icon e.g A[7:0] = 01000000b, turn ON icon ICS0 A[7:0] = 00111111b, turn OFF icon ICS63

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 0	94 A[7:6]	1 A_7	0 A_6	0 *	1 *	0 *	1 *	0 *	0 *	Set Icon ON / OFF Registers	A[7:6]: Icon register A[7:6] = 00b, turn OFF all icon A[7:6] = 01b, turn ON all icon A[7:6] = 11b, blink all icons
0 0	95 A[7:0]	1 *	0 *	0 A_5	1 A_4	0 *	1 A_2	0 A_1	1 A_0	Set Icon Blinking Cycle	A[2:0]: icon blinking cycle (RESET) 000 0.25sec 001 0.50sec 010 0.75sec 011 1.00sec (RESET) 100 1.25sec 101 1.50sec 110 1.75sec 111 2.00sec A[5:4]: icon OSC frequency, frequency increase as level increases [RESET = 11b] 00 61KHz 01 64KHz (RESET) 10 68KHz 11 73KHz **Note** [1] Blinking cycles is measured at 100Hz icon frame frequency and duty ratio of 50%
0 0	96 A[7:0]	1 A_7	0 A_6	0 A_5	1 A_4	0 *	1 A_2	1 A_1	0 A_0	Set Icon Duty	A[2:0]: Set icon AC drive 000 DC drive (RESET) 001 63 / 64 duty ratio 010 62 / 64 duty ratio 011 61 / 64 duty ratio 100 60 / 64 duty ratio 101 59 / 64 duty ratio 110 58 / 64 duty ratio 111 57 / 64 duty ratio A[7:4]: Set icon frame frequency **Note** [1] Icon frame frequency must NOT be set to 0000b

Fundamental Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 0	A0 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Re-map	Re-map setting in Graphic Display Data RAM (GDDRAM) A[7:0]: Remap [RESET = 00h] A[0] = 0, Disable Column Address Re-map (RESET) A[0] = 1, Enable Column Address Re-map A[1] = 0, Disable Nibble Re-map (RESET) A[1] = 1, Enable Nibble Re-map A[2] = 0, Enable Horizontal Address Increment (RESET) A[2] = 1, Enable Vertical Address Increment A[4] = 0, Disable COM Re-map (RESET) A[4] = 1, Enable COM Re-map A[6] = 0, Disable COM Split Odd Even (RESET) A[6] = 1, Enable COM Split Odd Even
0 0	A1 A[7:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	A[6:0]: Vertical scroll by setting the starting address of display RAM from 0 ~ 127 [RESET = 00h]
0 0	A2 A[7:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	A[6:0]: Set vertical offset by COM from 0 ~ 127 [RESET = 00h] e.g. Set A[6:0] to 010000b to move COM16 towards COM0 direction for 16 lines
0 0 0 0	A4 A5 A6 A7	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	Set Display Mode	A4: Normal display (RESET) A5: All ON (All pixels have gray scale of 15, GS15) A6: All OFF (All pixels have gray scale of 0, GS0) A7: Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, …)
0 0	A8 A[6:0]	0 *	0 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set MUX Ratio	A[6:0]: Set MUX ratio from 16MUX ~ 128MUX [RESET = 7Fh]
0 0	AE AF	1 1	0 0	1 1	0 0	1 1	1 1	1 1	0 1	Set Sleep mode ON / OFF	A[0] = 0, Sleep mode ON (The display is OFF) A[0] = 1, Sleep mode OFF (The display is ON)
0 0	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[7:0]: RESET and pre-charge phase length [RESET=53h] A[3:0] Phase 1 period of 1~16 DCLK's [RESET=3h] e.g. A[3:0] = 1111, 16 DCLK Clock A[7:4] Phase 2 period of 1~16 DCLK's [RESET=5h] e.g. A[7:4] = 1111, 16 DCLK Clocks

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0 0	B2 A[6:0]	1 *	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Frame Frequency	Set the frame frequency of the matrix display A[6:0]: Total number of DCLK's per row. Ranging from 14h to 4Eh DCLK's [RESET = 23h] Then the frame Frequency = DCLK freq /A[6:0].
0 0	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Front Clock Divider (DIVSET)/ Oscillator Frequency	A[3:0], DIVSET divided by DIVSET+1 (i.e. 1 to 16) [reset=00000b] A[7:4] OSC frequency, frequency increase as level increases [RESET = 0000b]
0	B7	1	0	1	1	0	1	1	1	Set Default Gray Scale Table	The default gray scale table is set in unit of DCLK's as follow: GS1 level Pulse width = 2 GS2 level Pulse width = 4 GS3 level Pulse width = 6 … … … GS13 level Pulse width = 26 GS14 level Pulse width = 28 GS15 level Pulse width = 30
0 0 0 … … … 0 0	B8 A1[5:0] A2[5:0] … … … A14[5:0] A155:0]	1 * * ... ... * *	0 * * ... ... * *	1 $A1_5$ $A2_5$ ... ... $A14_5$ $A15_5$	1 $A1_4$ $A2_4$ ... ... $A14_4$ $A15_4$	1 $A1_3$ $A2_3$ ... ... $A14_3$ $A15_3$	0 $A1_2$ $A2_2$ ... ... $A14_2$ $A15_2$	0 $A1_1$ $A2_1$ ... ... $A14_1$ $A15_1$	0 $A1_0$ $A2_0$ ... ... $A14_0$ $A15_0$	Look Up Table for Gray Scale Pulse width	The next 15 data bytes set the gray scale pulse width in unit of DCLK's. A1[5:0], value for GS1 level Pulse width A2[5:0], value for GS2 level Pulse width … … … A14[5:0], value for GS14 level Pulse width A15[5:0], value for GS15 level Pulse width **Note** [1] The pulse width value of GS1, GS2, ... , GS15 should not be equal. i.e. 0<GS1<GS2 … <GS15

Fundamental Command Table

D/C	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 0	BB A[3:0]	1 *	0 *	1 *	1 *	1 A_3	0 A_2	1 A_1	1 A_0	Ser Current Pre-charge Period	A[3:0]: Current pre-charge period 0000 0 DCLK 0001 1 DCLKs 0010 2 DCLKs : 0111 7 DCLKs (POR) : 1111 15 DCLKs
0 0	BC A[5:0]	1 *	0 *	1 A_5	1 A_4	1 A_3	1 A_2	0 A_1	0 A_0	Set Pre-charge voltage, V_P	A[5:0]: Pre-charge voltage [RESET = 0Fh] 000000 0.30 x V_{CC} 000001 0.31 x V_{CC} … ... … ... … ... 001111 0.45 x V_{CC} … ... … ... … ... 011111 0.63 x V_{CC} 1xxxxx 1.00 x V_{CC} or connect to V_{COMH} if V_{CC} > V_{COMH}
0 0	BE A[6:0]	1 *	0 A_6	1 A_5	1 A_4	1 A_3	1 A_2	1 A_1	0 A_0	Set V_{COMH}	A[6:0] : Output level high voltage for COM signal [RESET = 1Fh] 000000 0.51 x V_{CC} 000001 0.52 x V_{CC} … ... … ... 011110 0.82 x V_{CC} 011111 0.84 x V_{CC}
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A_2	0 1	1 0	Set Command Lock	A[2]: MCU protection status [RESET = 12h] A[2] = 0h, disable locking the MCU from entering command (RESET) A[2] = 1h, enable locking the MCU from entering command **Note** (1) Locking prohibits all commands and memory access

Table 9-2 : Read Command Table

(D/C#=0, R/W#(WR#)=1, E(RD#)=1 for 6800 or E(RD#)=0 for 8080)

$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D7=0:reserved D7=1:reserved D6=0:indicates the display is ON D6=1:indicated the display is OFF D5=0:reserved D5=1:reserved D4=0:reserved D4=1:reserved

Note

(1) Patterns other than that given in Command Table are prohibited to enter to the chip as a command; Otherwise, unexpected result will occur

9.1 Data Read / Write

To read data from the GDDRAM, input High to R/W#(WR#) pin and D/C# pin for 6800-series parallel mode, Low to E (RD#) pin and High to D/C# pin for 8080-series parallel mode.

In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data read. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read.

To write data to the GDDRAM, input Low to R/W#(WR#) pin and High to D/C# pin for 6800-series parallel mode and 8080-series parallel mode. For serial interface mode, it is always in write mode. In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data write. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data write.

It should be noted that, in horizontal address increment mode, the row address pointer would be increased by one automatically if the column address pointer wraps around. In vertical address increment mode, the column address pointer will be increased by one automatically if the row address pointer wraps around.

Table 9-3 : Address Increment Table (Automatic)

D/C#	R/W#(WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

10 COMMAND DESCRIPTIONS

10.1 Set Column Address (15h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

For example, column start address is set to 2 and column end address is set to 125, row start address is set to 1 and row end address is set to 126. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 125 and from row 1 to row 126 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation. Whenever the column address pointer finishes accessing the end column 125, it is reset back to column 2 and row address is automatically increased by 1. While the end row 126 and end column 125 RAM location is accessed, the row address is reset back to 1 and the column address is reset back to 2. The diagram below shows the way of column and row address pointer movement for this example.

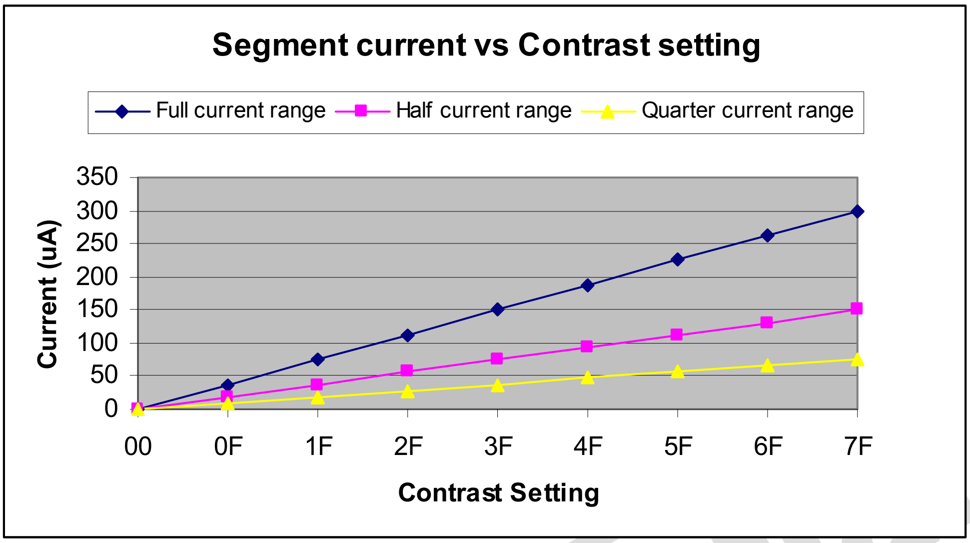
Figure 10-1 : Example of Column and Row Address Pointer Movement

	Col 0	Col 1	Col 2	…..	…….	Col125	Col126	Col127
Row 0								
Row 1								
Row 2								
: : :				: : :				
Row 125								
Row 126								
Row 127								

10.3 Set Contrast Current (81h)

This double byte command is to set Contrast Setting of the display. The chip has 128 contrast steps from 00H to 7FH. The segment output current increases linearly with the increase of contrast step

Figure 10-2 : Segment current vs Contrast setting



10.4 Set Pre-charge Current (82h)

This command is used to set the pre-charge current in the phase 3. The pre-charge current can be doubled to achieve faster pre-charging through seting 82h A[0]. Please refer to Table 9-1 : Command Table for the details of setting.

10.5 Set Master Icon Control (90h)

This double command is used to set the ON / OFF conditions of internal charge pump, icon circuits and overall icon status.

10.6 Set Icon Current Range (91h)

This double byte command is used to set one fix current range for all icons between the range of 0uA and 127 uA. The uniformity improved as the icon current range increases. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.7 Set Individual Icon Current (92h)

This double byte command is used to fine tune the current for each of the 64 icons. Command 92h followed by 64 single byte data have to be entered in order to make this command function. Below is the formula for calculating the icon current. Please also refer to Table 9-1 for detail information and breakdown levels of each step.

Icon Current = Single byte value / 127 x Maximum icon current set with above command 91h.

10.8 Set Individual Icon ON / OFF Registers (93h)

This double byte command is used to select one of the 64 icons and choose the ON, OFF or blinking condition of the selected icon.

10.9 Set Icon ON / OFF Registers (94h)

This double byte command is used to set the ON / OFF status of all 64 icons.

10.10 Set Icon Blinking Cycle (95h)

This double byte command is used to set icon oscillator frequency and blinking cycle selected with above command 93h. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.11 Set Icon Duty (96h)

This double byte command is used to set the icon frame frequency and icon AC drive duty ratio. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.12 Set Re-Map(A0h)

This double command has multiple configurations and each bit setting is described as follows:

- Column Address Remapping (A[0])

  This bit is made for increase the flexibility layout of segment signals in OLED module with segment arranged from left to right (when A[0] is set to 0) or from right to left (when A[0] is set to 1).

- Nibble Remapping (A[1])

  When A[1] is set to 1, the two nibbles of the data bus for RAM access are re-mapped, such that (D7, D6, D5, D4, D3, D2, D1, D0) acts like (D3, D2, D1, D0, D7, D6, D5, D4)

  If this feature works together with Column Address Re-map, it would produce an effect of flipping the outputs from SEG0-127 to SEG127-SEG0 as show in Table 8-7.

- Address increment mode (A[2])

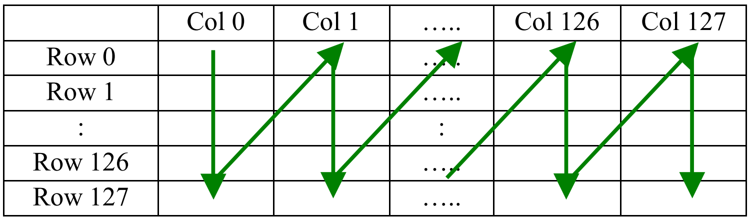
  When A[2] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 10-3.

Figure 10-3 : Address Pointer Movement of Horizontal Address Increment Mode

	Col 0	Col 1	…..	Col 126	Col 127
Row 0					
Row 1					
:	:	:	:	:	:
Row 126					
Row 127					

When A[2] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. if the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 10-4.

Figure 10-4 : Address Pointer Movement of Vertical Address Increment Mode



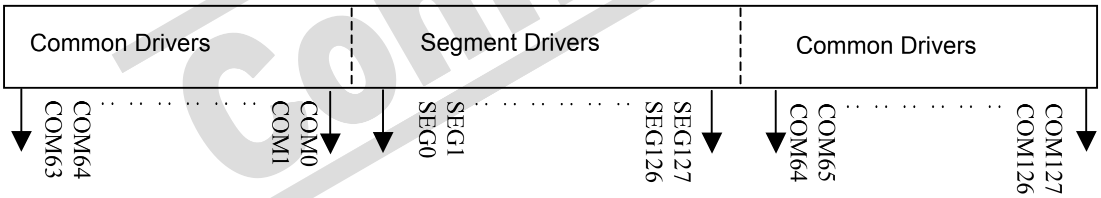
- COM Remapping (A[4])

  This bit defines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down (when A[4] is set to 0) or from bottom to up (when A[4] is set to 1). Table 8-8 shows one example of the using the COM Remapping to perform vertical scrolling.

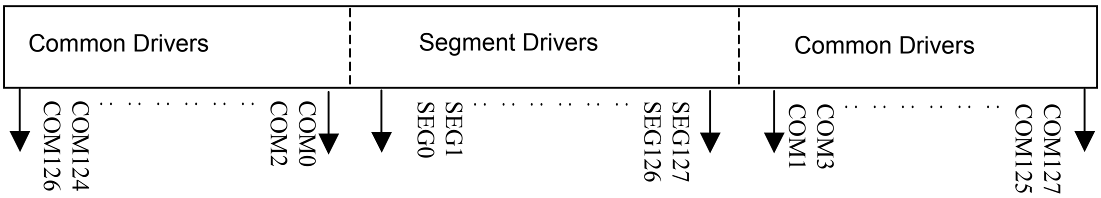
- Splitting of Odd / Even COM Signals (A[6])

  This bit is made to match the COM layout connection on the panel.

  When A[6] is set to 0, no splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below:
  COM127 → COM126 → … → COM 65 → COM64 → SEG127 → SEG126 → … → SEG1 → SEG0 → COM0 → COM1 → … → COM62 →COM63



When A[6] is set to 1, splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below :
COM127 → COM125 → … → COM 3 →COM1 → SEG127 →SEG126 → … →SEG1 → SEG0 →COM0 →COM2 →… →COM124 → COM126



10.13 Set Display Start Line (A1h)

This double byte command is to set Display Start Line register for determining the starting address of display RAM to be displayed by selecting a value from 0 to 127. Figure 10-5 shows an example using this command of this command when MUX ratio= 128 and MUX ratio= 126 and Display Start Line = 04h. In there, "ROW" means the graphic display data RAM row.

Figure 10-5 : Example of Set Display Start Line with no Remapping

	MUX ratio (A8h) = 128	MUX ratio (A8h) = 128	MUX ratio (A8h) = 126	MUX ratio (A8h) = 126
COM Pin	Display Start Line (A1h) = 0h	Display Start Line (A1h) = 4h	Display Start Line (A1h) = 0h	Display Start Line (A1h) = 4h
COM0	ROW0	ROW4	ROW0	ROW4
COM1	ROW1	ROW5	ROW1	ROW5
COM2	ROW2	ROW6	ROW2	ROW6
COM3	ROW3	ROW7	ROW3	ROW7
:	:	:	:	:
:	:	:	:	:
COM121	ROW121	ROW125	ROW121	ROW125
COM122	ROW122	ROW126	ROW122	ROW126
COM123	ROW123	ROW127	ROW123	ROW127
COM124	ROW124	ROW0	ROW124	ROW0
COM125	ROW125	ROW1	ROW125	ROW1
COM126	ROW126	ROW2	-	-
COM127	ROW127	ROW3	-	-

10.14 Set Display Offset (A2h)

This double byte command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-127. Figure 10-6 shows an example using this command when MUX ratio= 128 and MUX ratio= 126 and Display Offset = 04h. In there, "Row" means the graphic display data RAM row.

Figure 10-6 : Example of Set Display Offset with no Remapping

	MUX ratio (A8h) = 128	MUX ratio (A8h) = 128	MUX ratio (A8h) = 126	MUX ratio (A8h) = 126
COM Pin	Display Offset (A2h) = 0h	Display Offset (A2h) = 4h	Display Offset (A2h) = 0h	Display Offset (A2h) = 4h
COM0	ROW0	ROW4	ROW0	ROW4
COM1	ROW1	ROW5	ROW1	ROW5
COM2	ROW2	ROW6	ROW2	ROW6
COM3	ROW3	ROW7	ROW3	ROW7
:	:	:	:	:
:	:	:	:	:
COM121	ROW121	ROW125	ROW121	ROW125
COM122	ROW122	ROW126	ROW122	-
COM123	ROW123	ROW127	ROW123	-
COM124	ROW124	ROW0	ROW124	ROW0
COM125	ROW125	ROW1	ROW125	ROW1
COM126	ROW126	ROW2	-	ROW2
COM127	ROW127	ROW3	-	ROW3

10.15 Set Display Mode (A4h ~ A7h)

These are single byte commands and are used to set display status to Normal Display, Entire Display ON, Entire Display OFF or Inverse Display.

- Normal Display (A4h)
  Reset the above effect and turn the data to ON at the corresponding gray level.
- Set Entire Display On (A5h)
  Forces the entire display to be at gray scale level GS15, regardless of the contents of the display data RAM.
- Set Entire Display Off (A6h)
  Forces the entire display to be at gray scale level GS0, regardless of the contents of the display data RAM.
- Inverse Display (A7h)
  The gray scale level of display data are swapped such that “GS0” <-> “GS15”, “GS1” <-> “GS14”, etc.

10.16 Set MUX Ratio (A8h)

This double byte command sets multiplex ratio from 16 to 128. In RESET, multiplex ratio is 127.

10.17 Set Sleep Mode ON/OFF (AEh / AFh)

These single byte commands are used to turn the matrix display on the OLED panel display either ON or OFF. When the sleep mode is set to ON (AEh), the display is OFF, the segment and common output are in high impedance state and circuits will be turned off. When the sleep mode is set to OFF (AFh), the display is ON.

10.18 Set Phase Length (B1h)

In the second byte of this double command, lower nibble and higher nibble is defined separately. The lower nibble adjusts the phase length of Reset (phase 1). The higher nibble is used to select the phase length of pre-charge phase (phase 2). The phase length is ranged from 1 to 16 DCLK's.
RESET for A[3:0] is set to 3h which means 4 DCLK’s selected for Reset phase. RESET for A[7:4] is set to 5d which means 6 DCLK’s is selected for pre-charge phase. Please refer to Table 9-1 for detail breakdown levels of each step.

10.19 Set Frame Frequency (B2h)

This double byte command is used to set the number of DCLK’s per row between the range of 14h and 7Fh. Then the Frame frequency of the matrix display is equal to DCLK frequency / A[6:0].

10.20 Set Front Clock Divider / Oscillator Frequency (B3h)

This double command is used to set the frequency of the internal display clocks, DCLK's. It is defined by dividing the oscillator frequency by the divide ratio (Value from 1 to 16). Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency. The lower nibble of the second byte is used to select the oscillator frequency. Please refer to Table 9-1 for detail breakdown levels of each step.

10.21 Set Default Gray Scale Table (B7h)

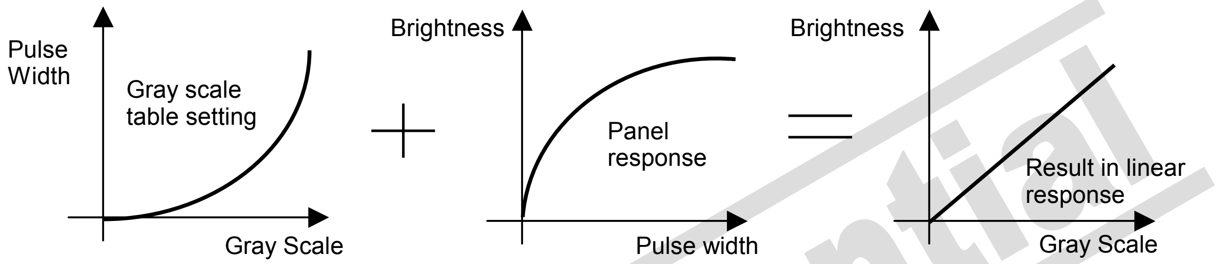
This single byte command is used to set the gray scale table to initial default setting.

10.22 Look Up Table for Gray Scale Pulse width (B8h)

This command is used to set each individual gray scale level for the display. Except gray scale level GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned on.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

Figure 10-7 : Example of gamma correction by gray scale table setting



10.23 Set Current Pre-charge period (BBh)

This double byte command is used to set the phase 3 current pre-charge period. The period of phase 3 can be programmed by command BBh and it is ranged from 0 to 15 DCLK's. Please refer to Table 9-1 : Command Table for the details of setting.

10.24 Set Pre-charge voltage, V_P (BCh)

This double byte command is used to set phase 2 pre-charge voltage level. It can be programmed to set the pre-charge voltage reference to V_{CC} or V_{COMH}. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.25 Set V_{COMH} (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH}. The level of V_{COMH} is programmed with reference to V_{CC}. Please refer to Table 9-1 for detail information and breakdown levels of each step.

10.26 No Operation (E3h)

This is a no operation command.

10.27 Set Command Lock (FDh)

This command is used to lock the MCU from accepting any command.

11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{DDIO}		-0.3 to +4.0	V
V_{CC}		0 to 18.0	V
V_{COMH}	Supply Voltage/Output voltage	0 to 16.0	V
-	SEG/COM output voltage	0 to 16.0	V
V_{in}	Input voltage	Vss-0.3 to Vdd+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

12 DC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}
V_{DD} = 2.4 to 3.5V
V_{CC} = 12V
V_{CI} = 3.5V
T_A = 25°C

Table 12-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage		9.0	12.0	16.0	V
V_{DD}	Logic Supply Voltage		2.4	3.0	3.5	V
V_{DDIO}	Power Supply for I/O pins		1.7	3.0	V_{DD}	V
V_{CI}	Charge Pump Supply Voltage		3.2	3.5	4.2	V
V_{ICON}	Icon Supply Voltage		6.4	7.0	8.4	V
V_{OH}	High Logic Output Level	I_{out} = 100uA, 3.3MHz	0.9 x V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low Logic Output Level	I_{out} = 100uA, 3.3MHz	0	-	0.1 x V_{DDIO}	V
V_{IH}	High Logic Input Level	I_{out} = 100uA, 3.3MHz	0.8 x V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low Logic Input Level	I_{out} = 100uA, 3.3MHz	0	-	0.2 x V_{DDIO}	V
$I_{DD, SLEEP}$	Sleep mode Current	V_{DD} = 3.0V, Display OFF, No panel attached	-5	0	5	uA
$I_{CC, SLEEP}$	Sleep mode Current	V_{DD} = 3.0V, Display OFF, No panel attached	-5	0	5	uA
I_{DD}	V_{DD} Supply Current	V_{DD} = 3.0V, Display ON, All 1's Contrast = 80h, No panel attached	50	TBD	80	uA
I_{CC}	V_{CC} Supply Current	V_{DD} = 3.0V, Display ON, All 1's Contrast = 80h, No panel attached	900	TBD	1100	uA
I_{DD}	V_{DD} Supply Current	V_{DD} = 3.0V, Display ON, All 0's Contrast = 80h, No panel attached	40	TBD	70	uA
I_{CC}	V_{CC} Supply Current	V_{DD} = 3.0V, Display ON, All 0's Contrast = 80h, No panel attached	210	TBD	250	uA
I_{SEG}	Segment Output Current Setting: V_{DD} = 3.0V, I_{REF} = 10uA, All 1's pattern, Display ON, Segment pin under test is connected with a 20KΩ resistive load to V_{SS}.	Contrast = FFh	290	TBD	350	uA
		Contrast = AFh	200	TBD	240	uA
		Contrast = 5Fh	110	TBD	130	uA
		Contrast = 0Fh	15	TBD	25	uA
Dev	Segment output current uniformity	Dev = $(I_{SEG} – I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN})/2$ I_{SEG}[0:127] = Segment current at contrast = FFh	-	-	±3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FFh)	Adj Dev = (I[n] - I[n+1]) / (I[n]+I[n+1])	-	±2.0	-	%
I_{CS}	Icon Segment Output Current Setting: V_{DD} = 3.0V, Icon Current Range = FFh, Individual Icon Current = 7Fh for all 64 icons. Icon segment pins under test is connected with a 20KΩ resistive load to V_{SS}.	V_{DD} = 3.0V, Display ON, No panel attached	120	TBD	140	uA
		V_{DD} = 3.0V, Display OFF, No panel attached	-5	0	5	uA

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Icon Dev	Icon Segment Output Current Uniformity	Dev = $(I_{SEG} – I_{MID})/I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN})/2$ $I_{SEG}[0:127]$ = Segment current at contrast = FFh	-	-	±3	%
Icon Adj. Dev	Adjacent pin output current uniformity	Adj Dev = (I[n] - I[n+1]) / (I[n]+I[n+1])	-	±2.0	--	%

13 AC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}
$V_{DD} = V_{DDIO} = 2.4$ to 3.5V
$V_{CC} = 9$ to 18V
$T_A = 25°C$

Table 13-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
FOSC[1]	Oscillation Frequency of Display Timing Generator	$V_{DD} = 3.0V$	-	3.0	-	MHz
FFRM	Frame Frequency for 128MUX Mode	128 x 128 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} X 1 / (D x K x N) [2]	-	Hz

Note
[1] Fosc stands for the frequency value of the internal oscillator
[2] D stands for divide ratio
K stands for total number of display clocks per row defined by command B2h
N stands for number of MUX selected by command A8h

Conditions:

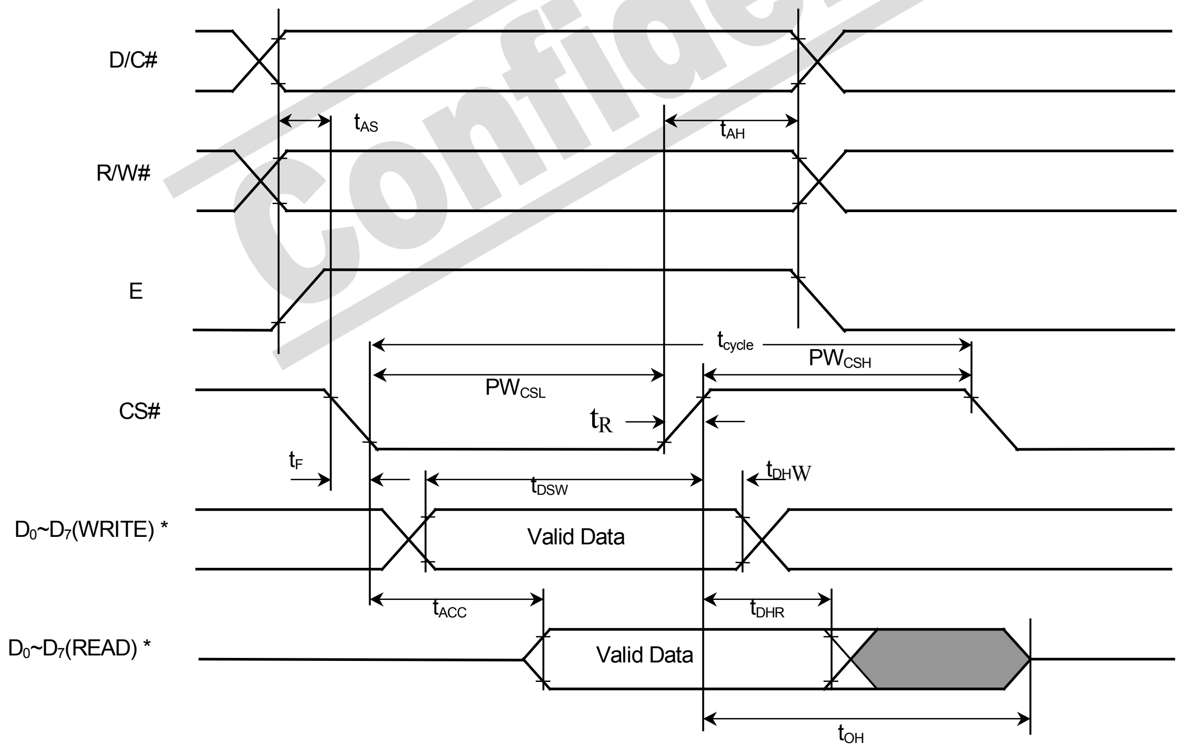
V_{DD} - V_{SS} = 2.4 to 3.5V

T_A = 25°C

Table 13-2 : 6800-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-1: 6800-series MPU parallel interface characteristics



Conditions:

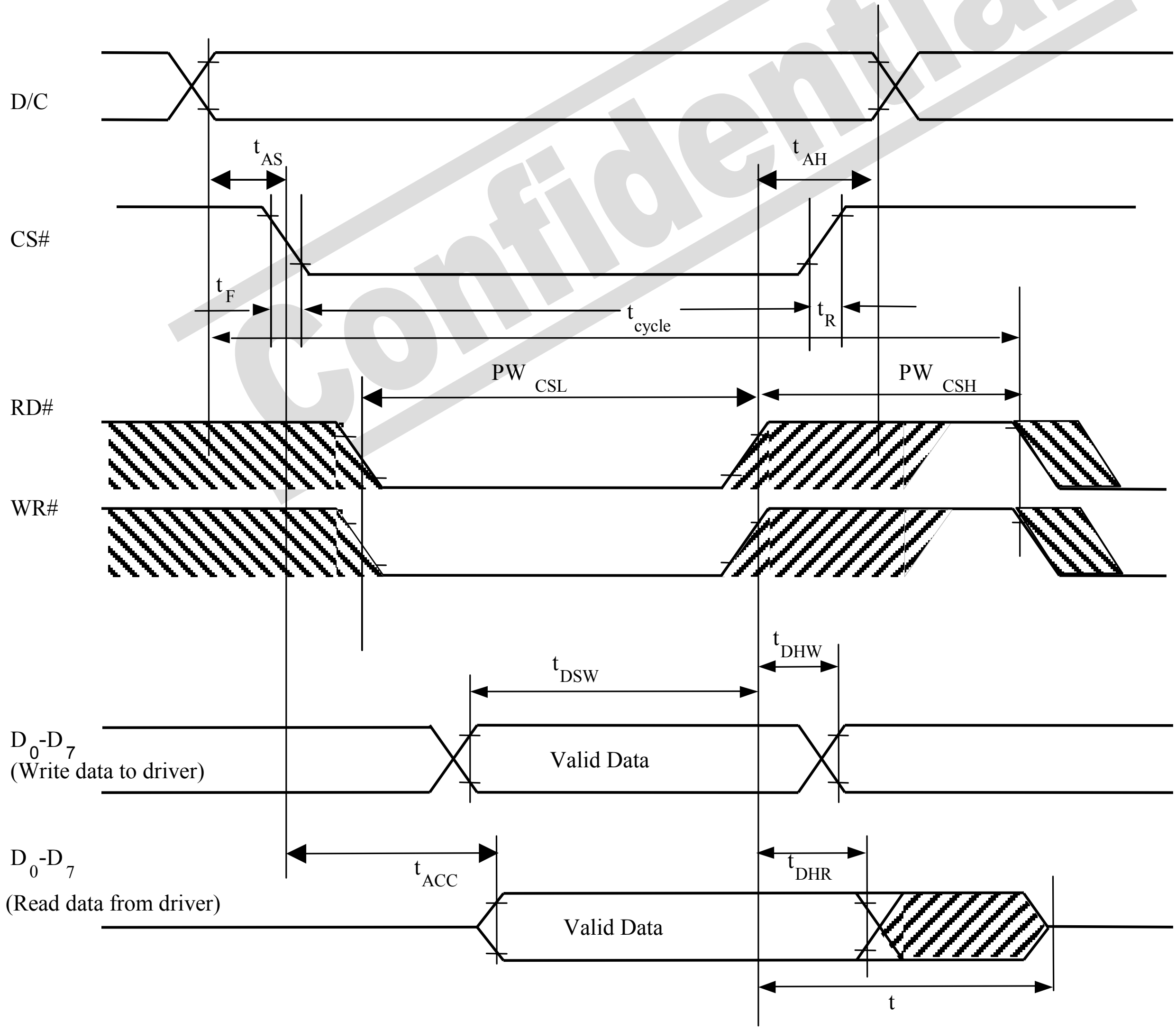
$V_{DD} - V_{SS}$ = 2.4 to 3.5V

T_A = 25°C

Table 13-3 : 8080-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-2 : 8080-series MPU parallel interface characteristics



Conditions:

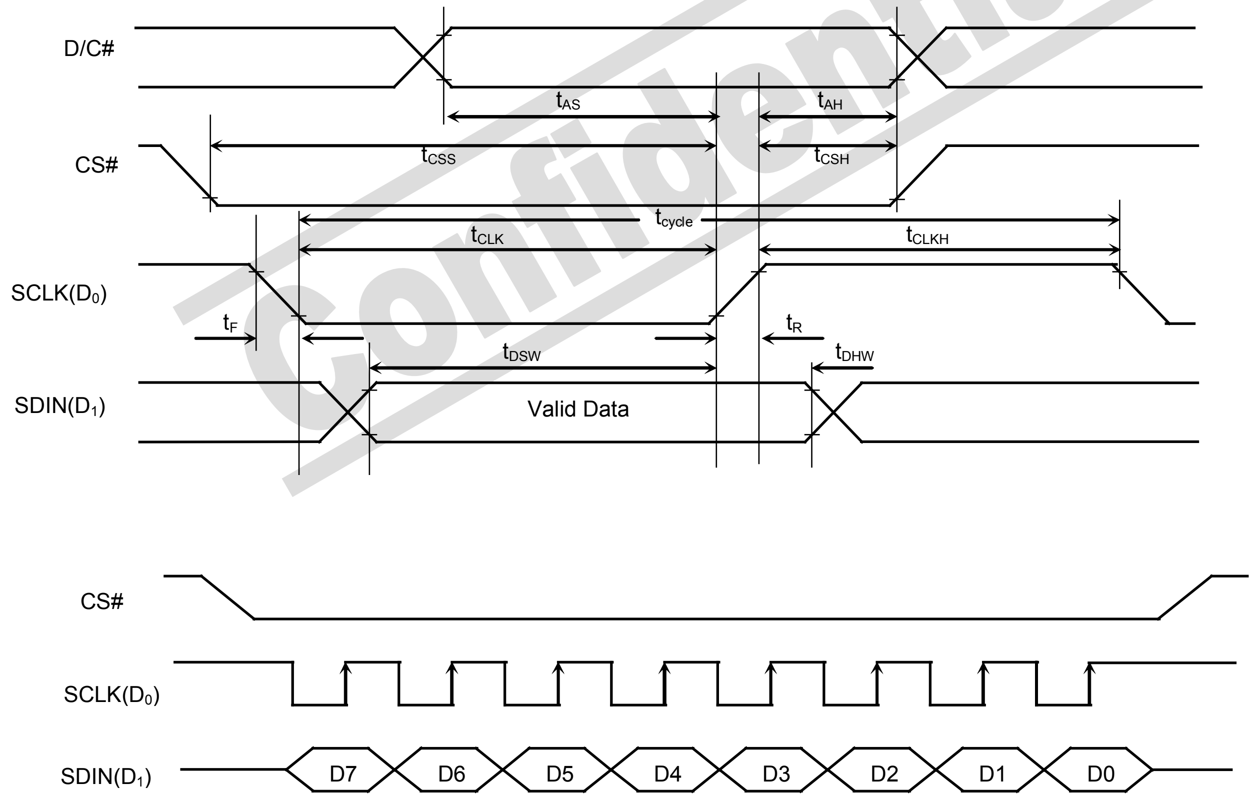
V_{DD} - V_{SS} = 2.4 to 3.5V

T_A = 25°C

Table 13-4 : Serial Interface Timing Characteristics

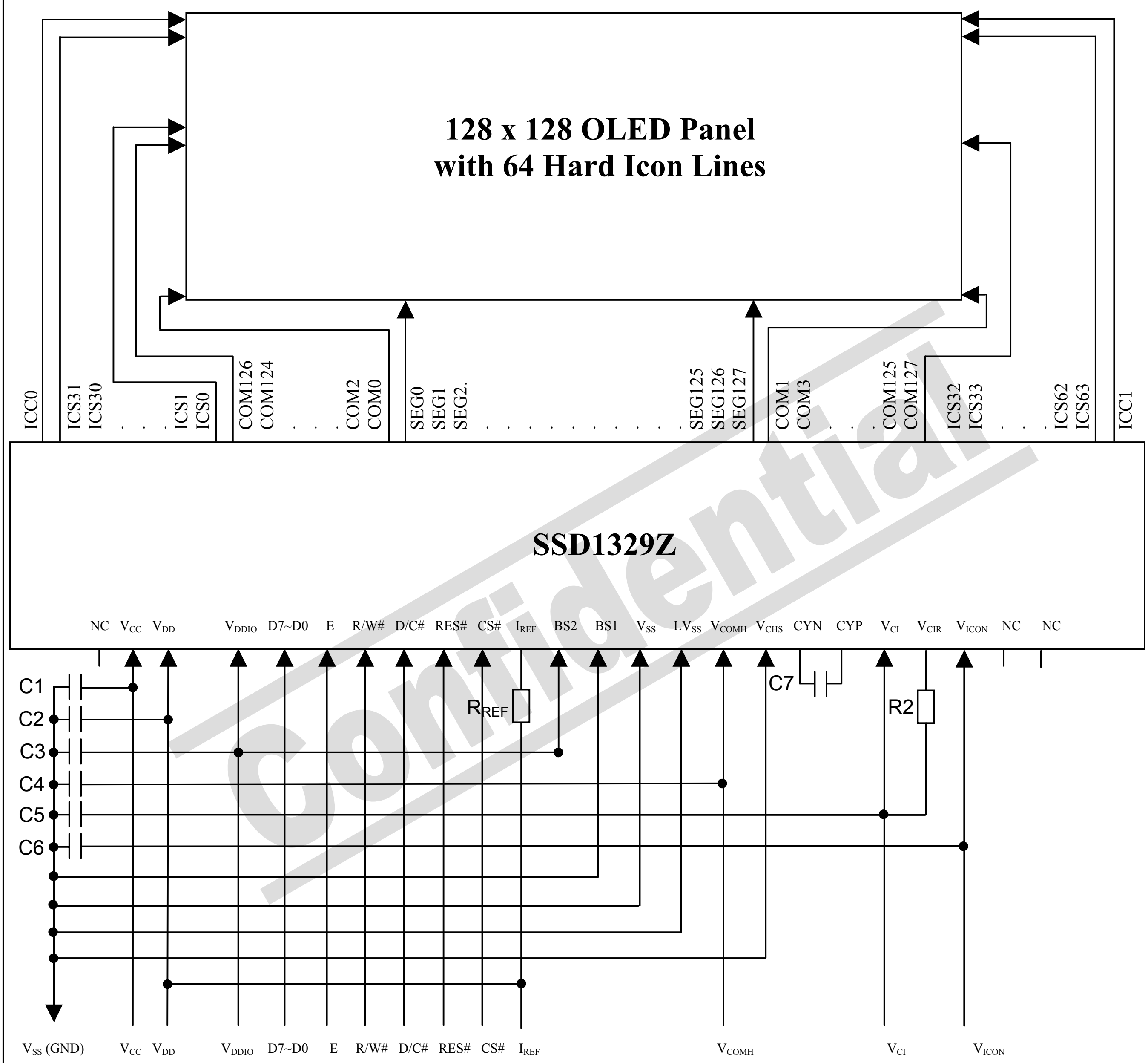
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 13-3 : Serial interface characteristics



14 APPLICATION EXAMPLES

Figure 14-1 : Application Example for SSD1329 8-bit 6800-parallel interface mode

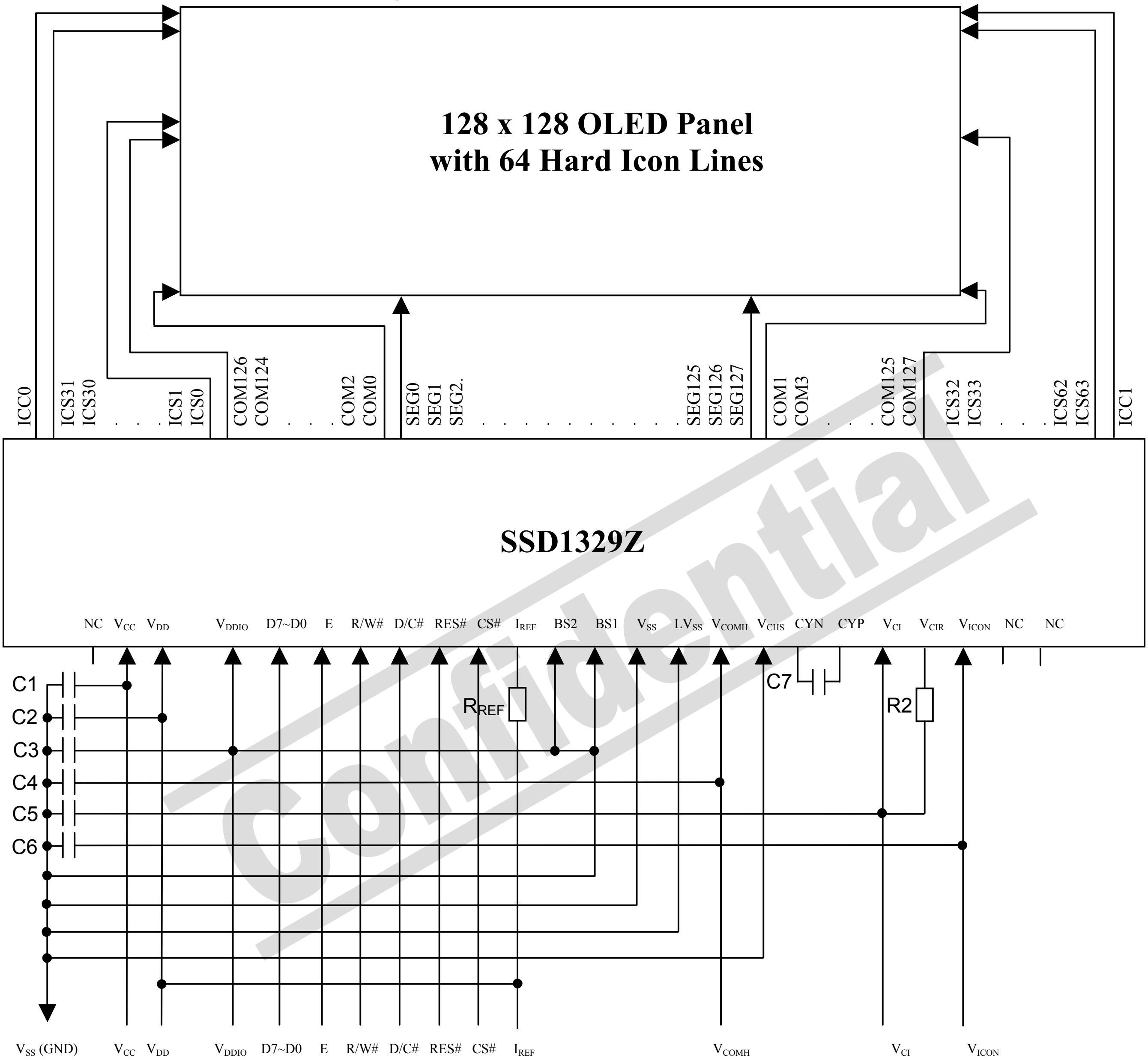


Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, RES#, CS#
Pin internally connected to VDDIO: CLS
Pin externally connected to VDDIO: BS2
Pin externally connected to VSS: LVSS, VCHS, BS0, BS1
Pin floated: GPIO0, GPIO1, TR0, TR1, TR2, TR3

$C_1 \sim C_5$ and C_7: 1uF in which C_1, C_4 have to be tantalum capacitors
C_6: 2uF in which C_6 has to be tantalum capacitor
Voltage at $I_{REF} = V_{DD} - 1.00V$
$R_{REF} = (V_{DD} - 1.00) / I_{REF} = (3.00 - 1.00)V / 10uA = 200K\Omega$
$R_2 = 33\Omega$

Figure 14-2 : Application Example for SSD1329 8-bit 8080-parallel interface mode

The configuration for 8-bit 8080-parallel interface mode, externally V_{CC} is shown in the following diagram: (V_{DD} = V_{DDIO} = 3.0V, V_{CC} = 12.0V, V_{CI} = 3.5V, I_{REF} = 10uA)

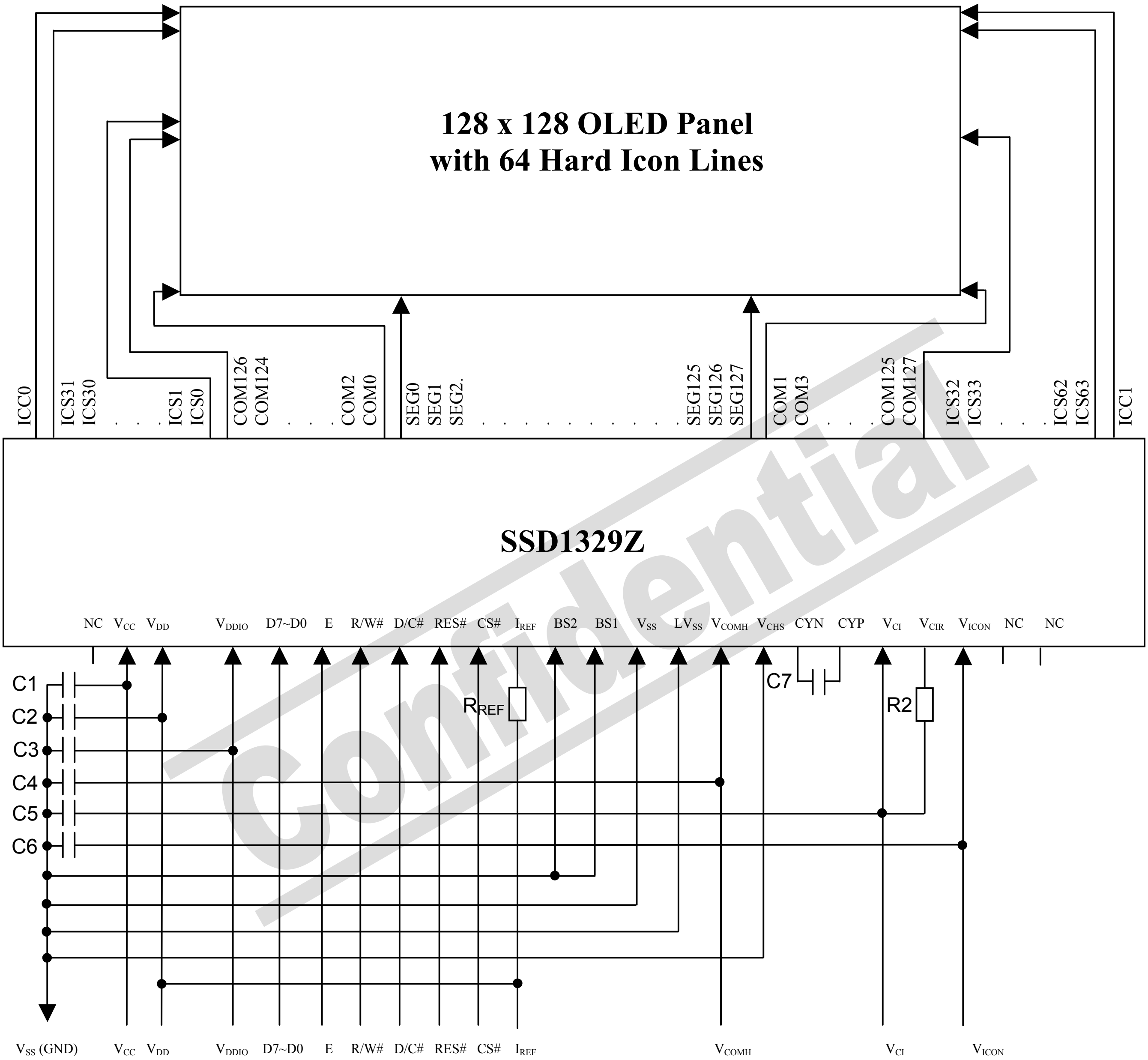


Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, RES#, CS#
Pin internally connected to VDDIO: CLS
Pin externally connected to VDDIO: BS2
Pin externally connected to VSS: LVSS, VCHS, BS0, BS1
Pin floated: GPIO0, GPIO1, TR0, TR1, TR2, TR3

C_1 ~ C_5 and C_7: 1uF in which C_1, C_4 have to be tantalum capacitors
C_6: 2uF in which C_6 has to be tantalum capacitor
Voltage at I_{REF} = V_{DD} – 1.00V
R_{REF} = (V_{DD} – 1.00) / I_{REF} = (3.00 – 1.00)V / 10uA = 200KΩ
R_2 = 33Ω

Figure 14-3 : Application Example for SSD1329 8-bit SPI-serial interface mode

The configuration for 8-bit SPI-serial interface mode, externally V_{CC} is shown in the following diagram: (V_{DD} = V_{DDIO} = 3.0V, V_{CC} = 12.0V, V_{CI} = 3.5V, I_{REF} = 10uA)

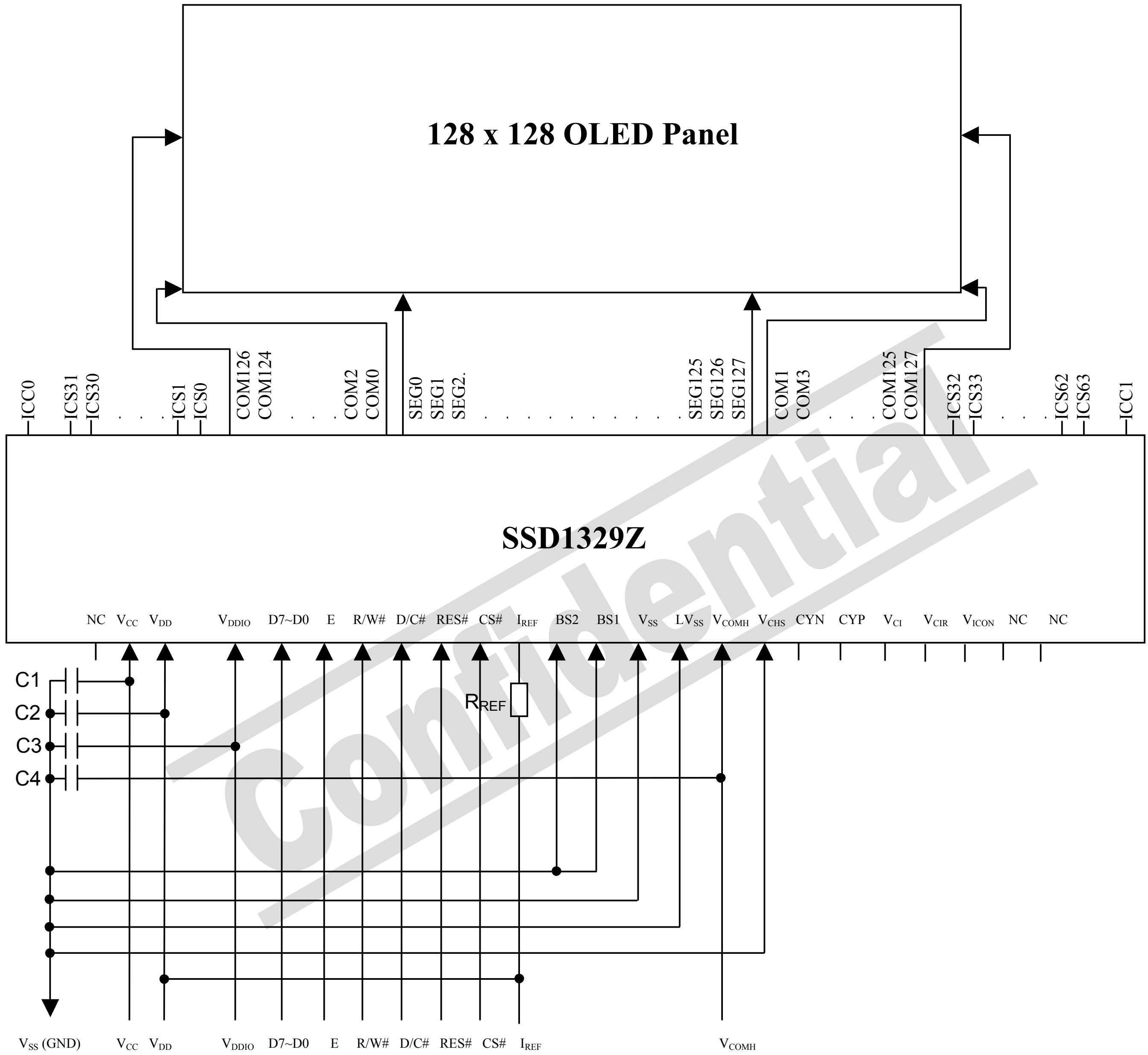


Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, RES#, CS#
Pin internally connected to VDDIO: CLS
Pin externally connected to VDDIO: BS2
Pin externally connected to VSS: LVSS, VCHS, BS0, BS1
Pin floated: GPIO0, GPIO1, TR0, TR1, TR2, TR3

C_1 ~ C_5 and C_7: 1uF in which C_1, C_4 have to be tantalum capacitors
C_6: 2uF in which C_6 has to be tantalum capacitor
Voltage at I_{REF} = V_{DD} – 1.00V
R_{REF} = (V_{DD} – 1.00) / I_{REF} = (3.00 – 1.00)V / 10uA = 200KΩ
R_2 = 33Ω

Figure 14-4 : Application Example for SSD1329 when hard icons are not used.

The configuration for 8-bit SPI-serial interface mode, externally V_{CC} is shown in the following diagram: (V_{DD} = V_{DDIO} = 3.0V, V_{CC} = 12.0V, I_{REF} = 10uA)



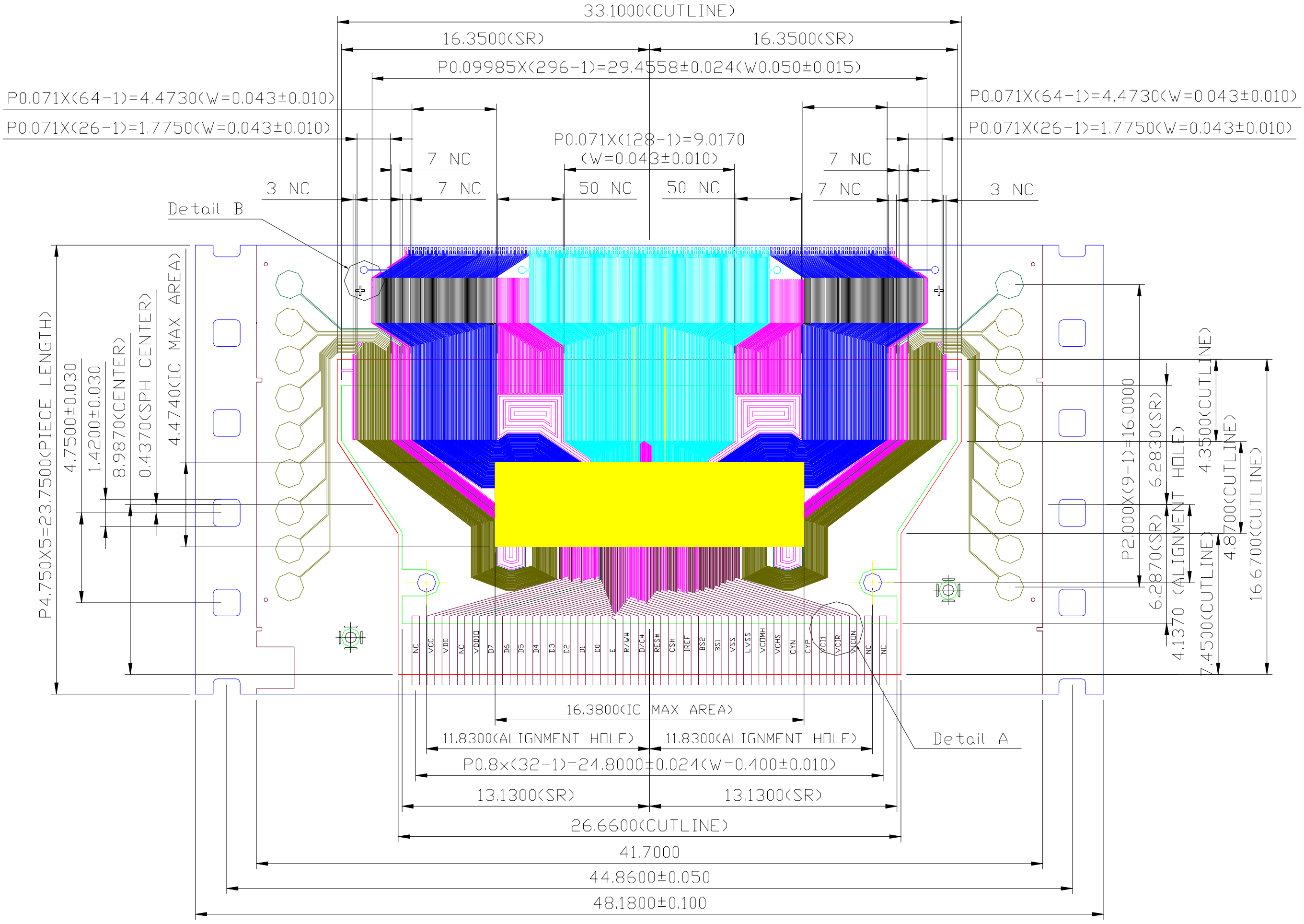
Pin connected to MCU interface: D0~D7, E, R/W#, D/C#, RES#, CS#
Pin internally connected to VDDIO: CLS
Pin externally connected to VDDIO: BS2
Pin externally connected to VSS: LVSS, VCHS, BS0, BS1
Pin floated: GPIO0, GPIO1, TR0, TR1, TR2, TR3

C_1 ~ C_5 and C_7: 1uF in which C_1, C_4 have to be tantalum capacitors
C_6: 2uF in which C_6 has to be tantalum capacitor
Voltage at I_{REF} = V_{DD} – 1.00V
R_{REF} = (V_{DD} – 1.00) / I_{REF} = (3.00 – 1.00)V / 10uA = 200KΩ
R_2 = 33Ω

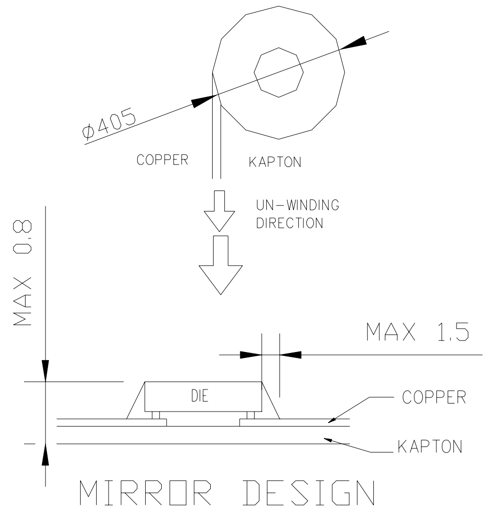
15 PACKAGE INFORMATION

15.1 SSD1329UR1 Detail Dimension

Figure 15-1 : SSD1329UR1 detail dimension

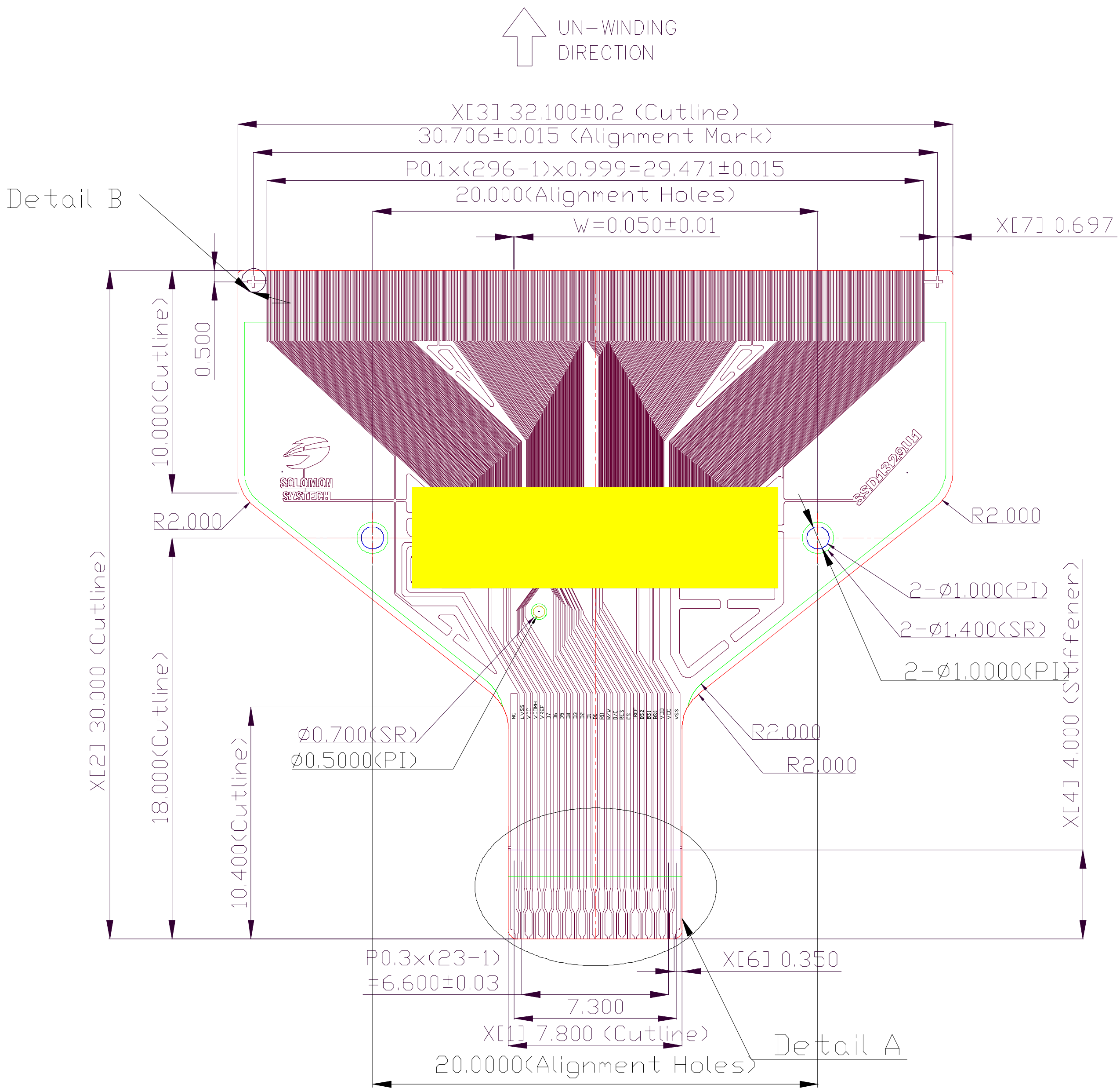


NOTE:
1. GENERAL TOLERANCE: ±0.05mm
2. CUTLINE TOLERANCE: ±0.15mm
3. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 15±10um
4. SN PLATING: 0.20±0.05um

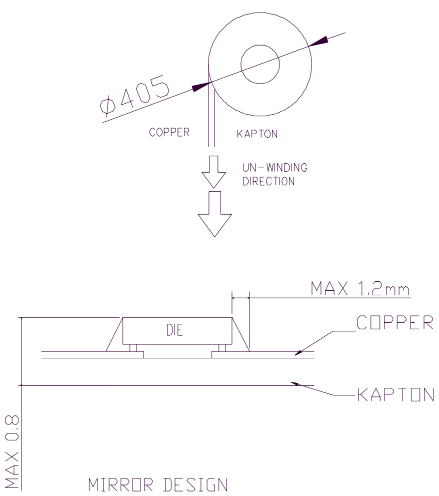


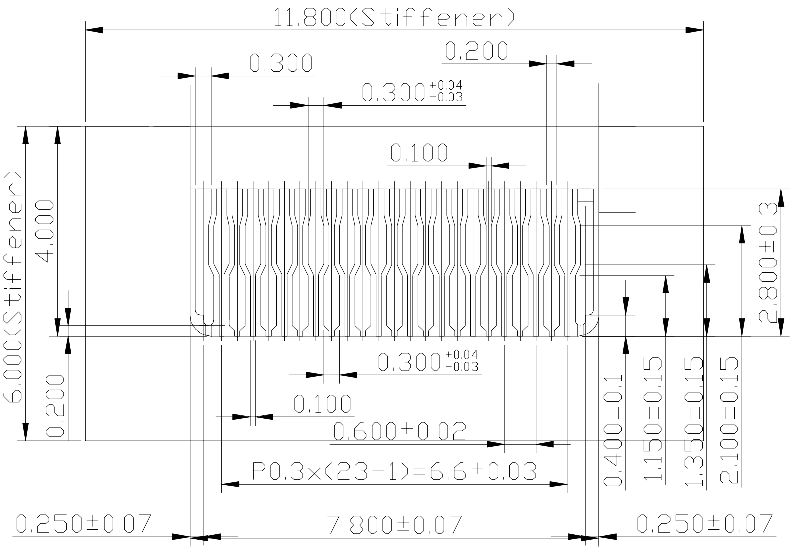
15.2 SSD1329U1 Detail Dimension

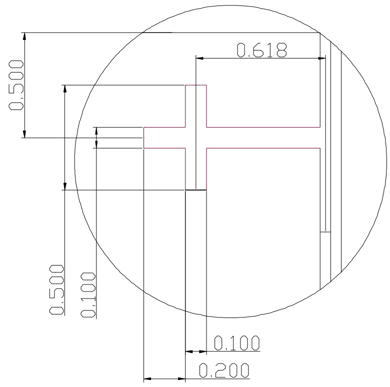
Figure 15-2 : SSD1329U1 detail dimension



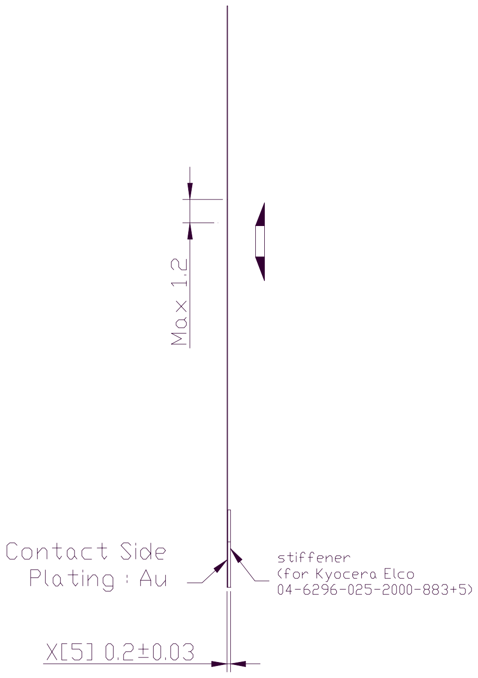
NOTE:
1. GENERAL TOLERANCE: ±0.05MM
2. MATERIAL
   PI: 38±4UM
   CU: 8±2UM
   SR: 15±10UM , SR TOLERANCE±0.2
3. AU/Ni PLATING: AU 0.4±0.1UM
   Ni 0.5±0.1UM
4. TAPSITE: 8 SPH, 38MM







Detail B
Scale : 10x
Tolerance:±0.03



http://www.solomon-systech.com