HIGH-VOLTAGE MIXED-SIGNAL IC

UC1603

68COM x 98SEG Matrix LCD Controller-Driver

ES Specifications
Revision 0.6

April 27, 2007

ULTRACHIP

The Coolest LCD Driver, Ever!!

Table of Content

UC1603

Single-Chip, Ultra-Low Power
68COM x 98SEG Matrix
Passive LCD Controller-Driver

INTRODUCTION

UC1603 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power COM and SEG drivers, UC1603 contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation, and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 68x98 graphics STN LCD panels.
- Support both row-ordered and column-ordered display buffer RAM access.
- Support industry standard 8-bit parallel bus (8080 and 6800 modes), 4-wire, 3-wire, and 2-wire serial buses (S8, S9, and I^2C).
- Ultra-low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display, Bias Ratio and Frame Rate allow many flexible power management options
- Software programmable frame rates at 80 and 100 Hz.
- Four software programmable temperature compensation coefficients
- Self-configuring 7-x charge pump with on-chip pumping capacitors. Only 3 external capacitors to operate.
- On-chip bypass capacitor for V_{LCD} makes V_{LCD} bypass capacitor optional.
- On-chip Power-ON Reset and Software RESET commands, make RST pin optional.
- Very low pin count (9~10-pin) allows exceptional image quality in COG format on conventional ITO glass.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- V_{DD} (digital) range (Typ.) : 1.8V~ 3.3V
  V_{DD} (analog) range (Typ.) : 2.6V ~ 3.3V
  LCD V_{OP} range: 4.8V ~ 11.5V
- Software programmable 4 temperature compensation coefficients.
- Available in gold bump dies
- COM/SEG bump information
  Bump pitch (COM and SEG) : 32.5 μM
  Bump gap : 13 μM
  Bump surface : 2008.5 μM^2

ORDERING INFORMATION

Part Number	I^2C	Description
UC1603iGAA	Yes	Gold Bumped Die

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I^2C

The implementation of I^2C is already included and tested in all silicon. However, unless I^2C licensing obligation is executed satisfactorily, it is not legal to use UltraChip product for I^2C applications. Unless I^2C version is ordered from UltraChip, the customer will take the responsibility for all such licensing liabilities.

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LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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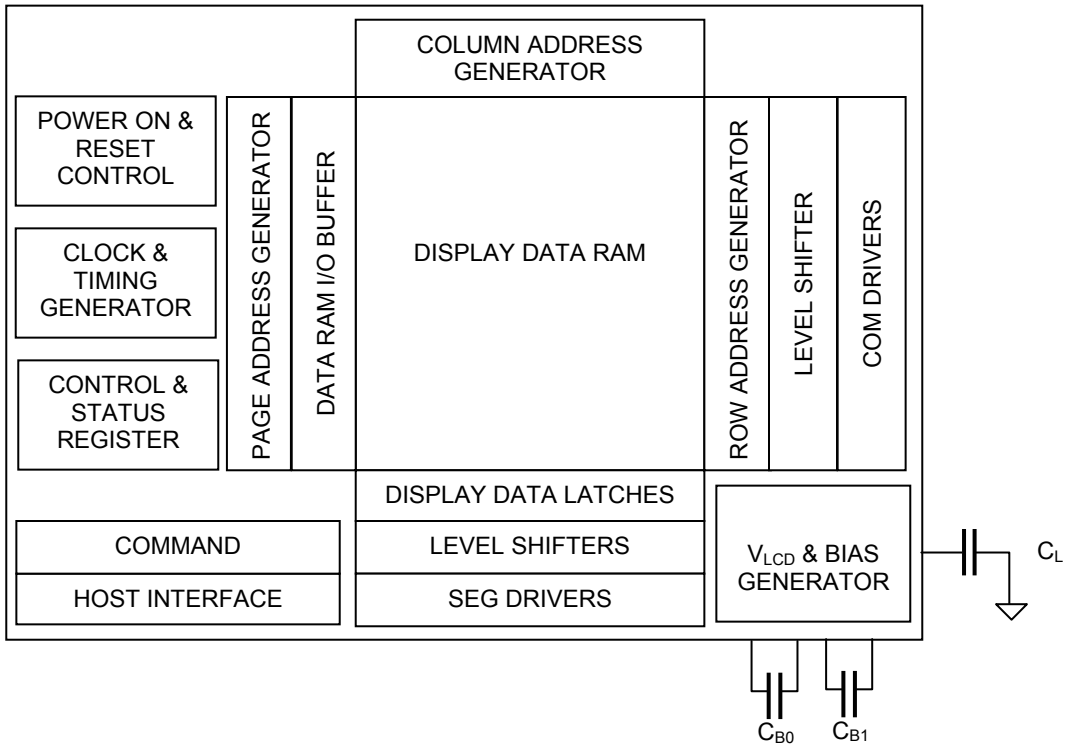
BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Pins	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	2 2 2	V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	4 3	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for V_{SS} and V_{SS2}.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B1+} V_{B1-} V_{B0+} V_{B0-}	PWR	2 2 2 2	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimizing the trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT}	PWR	1 2	Main LCD Power Supply. When internal V_{LCD} is used, connect these pins together. When external V_{LCD} source is used, connect external V_{LCD} source to V_{LCDIN} pins and leave V_{LCDOUT} open. By-pass capacitor C_L is optional. It can be connected between V_{LCD} and V_{SS}. When C_L is used, keep the trace resistance under 100 Ω.

NOTE

- Recommended capacitor values:
  C_B: 150x ~ 250x LCD load capacitance or 2.2μF (5V), whichever is higher.
  C_L: 330nF (25V) is appropriate for most applications.

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>1
1</td><td>Bus mode. The interface bus mode is determined by BM.
<table>
<tr><th>BM[1:0]</th><th>D[7]</th><th>Mode</th></tr>
<tr><td>11</td><td>Data</td><td>6800/8-bit</td></tr>
<tr><td>10</td><td>Data</td><td>8080/8-bit</td></tr>
<tr><td>01</td><td>1</td><td>I^2C</td></tr>
<tr><td>01</td><td>0</td><td>3-wire SPI w/ 9-bit token
(S9: conventional)</td></tr>
<tr><td>00</td><td>0</td><td>4-wire SPI w/ 8-bit token
(S8: conventional)</td></tr>
</table></td></tr>
<tr><td>CS0 / A2
CS1 / A3</td><td>I</td><td>1
1</td><td>Chip Select or Chip Address. In S8 and S9 modes, chip is selected when CS0=”L” and CS1=”H”. When the chip is not selected, D[1:0] will be high impedance.
In I^2C mode, these two pins specifies bits 3~2 of 1603’s device address (A[3:2]).</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1603 has built-in Power-On Reset and Software Reset command, RST pin is not required for proper chip operation.
An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select the incoming command if it is a control instruction or for display data. CD pin is not used in S9 mode. Connect it to V_{DD} or V_{SS} then.
”L”: control instruction ”H”: display data</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR[1:0] controls the read/write operation of the host interface. See Section Host Interface for more detail.
In parallel mode, the meaning of WR[1:0] depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td>8</td><td>Bi-directional bus for both serial host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA.
<table>
<tr><th></th><th>BM=1x
(8-bit)</th><th>BM=01
(I^2C)</th><th>BM=01
(S9)</th><th>BM=00
(S8)</th></tr>
<tr><td>DB0</td><td>D0</td><td>SCK</td><td>SCK</td><td>SCK</td></tr>
<tr><td>DB1</td><td>D1</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB2</td><td>D2</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB3</td><td>D3</td><td>SDA</td><td>SDA</td><td>SDA</td></tr>
<tr><td>DB4</td><td>D4</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB5</td><td>D5</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB6</td><td>D6</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>DB7</td><td>D7</td><td>1</td><td>0</td><td>0</td></tr>
</table>
Connect any unused pins to V_{SS}.</td></tr>
</table>

Name	Type	Pins	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG98	HV	98	SEG (column) driver outputs. Support up to 98 pixels. Leave unused driver outputs open.
COM1 ~ COM64	HV	68	COM (row) driver outputs. Support up to 64 rows. When designing LCM, always start from COM1. If the LCM has *N* pixel rows and *N* is less than 64, set CEN to be *N-1*, and leave COM drivers [N+1 ~ 64] open-circuit.
CIC	HV	4	Icon driver outputs. Leave it open if not used.
MISC. PINS			
V_{SSX}	O	2	Auxiliary V_{SS}. These pins are connected to the main V_{SS} bus within the IC. These pads are provided to facilitate chip configurations in COG application. These pins should *NOT* be used to provide V_{SS} power to the chip. It is not necessary to connect V_{SSX} to main V_{SS} externally.
TST4	I	1	Test control. Connect to GND.
TST1~2	I/O	1	Test I/O pins. Leave these pins open during normal use.

Note: Several control registers will specify the "0-based index" for COM and SEG electrodes. In those situations, COM*x* or SEG*x* will correspond to index *x*-1, and the value range for those index registers will be 0~67 for COM and 0~97 for SEG.

RECOMMENDED COG LAYOUT

(TBD)

NOTES FOR V_{DD} WITH COG:

The minimum operation condition of UC1603, V_{DD}=1.65V, should be met under all operating conditions. Unless V_{DD} and $V_{DD2/3}$ ITO trances can each be controlled to be 20Ω or lower; otherwise V_{DD}-$V_{DD2/3}$ separation can cause the actual on-chip V_{DD} to drop below V_{DD}=1.8V during high speed Data Write condition. Therefore, for COG, V_{DD}-$V_{DD2/3}$ separation requires very careful ITO layout and very stringent testing before MP.

CONTROL REGISTERS

UC1603 contains registers that control the operation of the chip. These registers can be modified by software commands. The commands supported by UC1603 are described in the next section. The following table is a summary of all the registers defined by UC1603 and their default values.

Name: Symbolic reference of the register.
Bits: Number of bits in this register.
Default: Register value after the chip power up or system reset. The bold numbers show these defaults.
Description: Register meaning and functions.

Name	Bits	Default	Description
SL	7	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (67). Setting SL outside of this range causes undefined effect on the displayed image. SL will affect icon output CIC.
CA	7	00H	Column Address of Display Data RAM (DDRAM). Value range is **0**~97. (Used to access DDRAM access from Host Interface)
PA	4	00H	Page Address of DDRAM (**0** ~ 8) (Used in Host to access DDRAM)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00: 6 01: 7 10: 8 **11: 9**
TC	2	0H	Temperature Compensation (per ^{o}C). **00b: 0.00%** 01b: -0.05% 10b: -0.10% 11b: -0.15%
PM	8	99H	Electronic Potentiometer to fine tune the value of V_{LCD}.
PC	3	6H	Power Control. PC[0]: **0b: LCD ⩽ 11nF** 1b: LCD: 12 ⩽ LCD ⩽ 20nF PC[2:1]: 00b: External V_{LCD} **11b: Internal V_{LCD}** (7x charge pump)
AC	3	1H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (**Default 1: ON**) AC[1]: Auto-Increment order **0: Page_C (CA) first** 1: Row (RA) first AC[2]: PID: RA (row address) auto Increment Direction (**L: +1** H: -1)
DC	3	0H	Display Control: DC[0]: PXV: Pixels Inverse (bit-wise data inversion. Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) When DC[2] is set to 0, the IC will enter Sleep mode.
LC	6	0H	LCD Control: LC[1:0]: Reserved. LC[2]: MX, Mirror X. SEG/Column sequence inversion (Default: **0 - OFF**) LC[3]: MY, Mirror Y COM/Row sequence inversion (Default: **0 - OFF**) LC[4]: Frame-Rate **0b: 80 fps** 1b: 100 fps (fps: frame per second) LC[5]: Partial Display **0b: Disable**. Mux-Rate = CEN+1 (DST and DEN are not used.) 1b: Enable. Mux-Rate = DEN – DST +1

Name	Bits	Default	Description
CEN DST DEN	7 7 7	43H 00H 43H	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = (the actual number of pixel rows on the LCD) – 1 CEN ⩾ DEN ⩾ DST + 9
APC0~1	8x2	N/A	Advanced Program Control. For UltraChip only. Please do NOT use.
STATUS REGISTER			
OM	2	–	Operating Modes (read only) 00: Reset 01: (Not used) 10: Sleep 11: Normal

COMMAND TABLE

The following is a list of host commands supported by UC1603

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
Useful Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	1	1	1	1	1	1	1	1	Read 1 byte	N/A
3	Get Status	0	1	MX	MY	WA	DE	Prod_ code		0	Ver	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA [3:0]	0H
	Set Column Address MSB	0	0	0	0	0	1	-	#	#	#	Set CA[6:4]	0H
5	Set Temp. Compensation	0	0	0	0	1	0	0	-	#	#	Set TC[1:0]	00b: 0.00%/°C
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[2:0]	6H
7	Set Adv. Program Control (double-byte command)	0	0	0 #	0 #	1 #	1 #	0 #	0 #	R #	R #	Set APC[R][7:0], R = 0~3	N/A
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	0	#	#	#	Set SL[6:4]	0H
9	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set RA[3:0]	0H
10	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set PM[7:0]	99H
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[5]	0b
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13	Set Frame Rate	0	0	1	0	1	0	0	0	0	#	Set LC[4]	0b: 80fps
14	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
15	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
16	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
17	Set LCD Mapping Control	0	0	1	1	0	0	#	#	0	0	Set LC[3:2]	0H
18	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
19	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
20	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
				#	#	#	#	#	#	#	#		
21	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 9
22	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	67 (=43H)
				-	#	#	#	#	#	#	#		
23	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	00H
				-	#	#	#	#	#	#	#		
24	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	67 (=43H)
				-	#	#	#	#	#	#	#		
Serial Read Command (Enabled only in S8/S9 mode)													
25	Get Status	0	0	1	1	1	1	1	1	1	0	Get status till chip disabled	N/A
		0	1	MX	MY	WA	DE	Prod_ code		0	Ver		

* Other than commands listed above, all other bit patterns may result in NOP (No Operation).

COMMAND DESCRIPTION

1. Write Data Byte to Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit Data write to SRAM							

2. Read Data Byte from Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit Data read from SRAM							

Write/Read Data Byte (Command 1, or 2) accesses Display Data RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increase or decrease automatically after each bus cycle, depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of the page, and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches the end of the page, CA will be reset to 0 and PA will increase or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM, PA will be wrapped around to the other end of RAM and continue. (See command `Window Programming` for more details)

3. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	MX	MY	WA	DE	Prod_Code		0	Ver

Status flag definitions:

MX: Status of register LC[0], mirror X.
MY: Status of register LC[1], mirror Y.
WA: Status of register AC[0]. Automatic column/row wrap around.
DE: Display enable flag. Display is enabled when DE=1.
Prod_Code: Production Identification. Default: 00b
Ver: IC Version. **0** or 1.

4. Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address LSB CA[6:4]	0	0	**0**	**0**	**0**	**1**	**-**	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA value range: **0**~97

5. Set Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b= -0.00%/ °C 01b= -0.05%/ °C 10b= -0.10%/ °C 11b= -0.15%/°C

6. Set Power Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Multiplexing Rate PC[2:0]	0	0	**0**	**0**	**1**	**0**	**1**	PC2	PC1	PC0

Set PC[0] according to the capacitance loading of LCD panel.

0b: LCD: ≤ 12nF 1b: LCD: 12~20nF

Set PC[2:1] to program the build-in charge pump stages:

00b: External V_{LCD} **11b: Internal V_{LCD}** (7x charge pump)

7. Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control APC[R][7:0] (Double-byte command)	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	R
	0	0	APC register parameter							

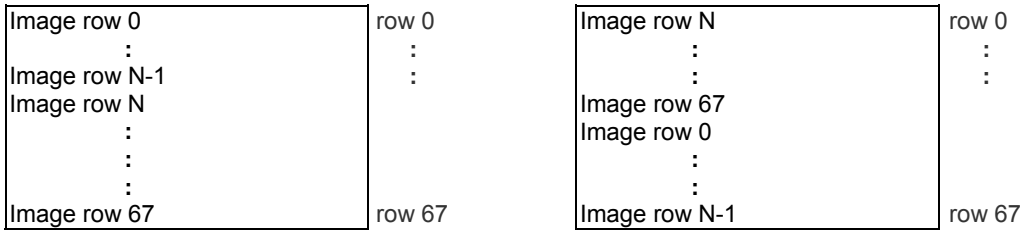
For UltraChip only. Please Do *NOT* use.

8. Set Scroll Line

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	**0**	**1**	**0**	**1**	**0**	SL6	SL5	SL4

Set the scroll line number. Possible value = **0**~67

Scroll line setting will scroll the displayed image up by *SL* rows.



This `Set Scroll Line` command will also affected the icon output, CIC.

9. Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address PA[3:0]	0	0	**1**	**0**	**1**	**1**	PA3	PA2	PA1	PA0

Set the SRAM page address before write/read memory from host interface. Each page of SRAM corresponds to 8 COM lines on LCD panel, except for the last page. The last page corresponds to the icon output CIC.

Possible value = **0**~8.

10. Set V_{BIAS} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer PM [7:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM							

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: 0 ~ 255

11. Set Partial Display Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LC [5]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**0**	LC5

This command is used to enable partial display function.

L[5]: **0b Disable Partial Display**, Mux-Rate = CEN+1 (DST,DEN not used.)
1b Enable Partial Display, Mux-Rate = DEN – DST+1

12. Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control. It controls the auto-increment behavior of CA and PA.

AC[0] - WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will reset to 0, and PA or CA will increase by one.

AC[1] – Auto-Increment order
0 : column (CA) increment (+1) first until CA reach CA boundary, then PA will increase by (+/-1).
1 : page (PA) increment (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

AC[2] – PID, page address (PA) auto increment direction (**0**/1 = **+**/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether page address will be adjusted by +1 or –1.

13. Set Frame Rate

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Frame Rate LC [4]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	LC4

Program LC [4] for frame rate setting

0b: 80 fps 1b: 100 fps
(fps: frame per second)

14. Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

15. Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

16. Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	DC2

This command is for programming register DC[2]. When DC[2] is set to 1, UC1603 will first exit from sleep mode, restore the power and then turn on COM drivers and SEG drivers.

17. Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Control LC[3:2]	0	0	**1**	**1**	**0**	**0**	MY	MX	**0**	**0**

Set LC[3:2] for COM (row) mirror (MY), SEG (column) mirror (MX).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 97-CA and inversing each byte as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

18. System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset.

Control register values will be reset to their default values. Data store in RAM will not be affected.

19. NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

20. Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(Double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do *NOT* use.

21. Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:
00b= 6 01b= 7 10b= 8 **11b= 9**

22. Set COM End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN [6:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	**-**	CEN register parameter						

This command programs the ending COM electrode.

CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-row in the LCD. When the LCD has less than 67 pixel rows, the LCD designer should set CEN to n-1 (where n is the number of pixel rows) and use COM(1) through COM(n) as COM driver electrodes.

23. Set Partial Display Start

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST [6:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(Double-byte command)	0	0	**-**	DST register parameter						

This command programs the starting COM electrode. Which gas been assigned a full scanning period and will output an active COM scanning pulse.

24. Set Partial Display End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN [6:0]	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(Double-byte command)	0	0	**-**	DEN register parameter						

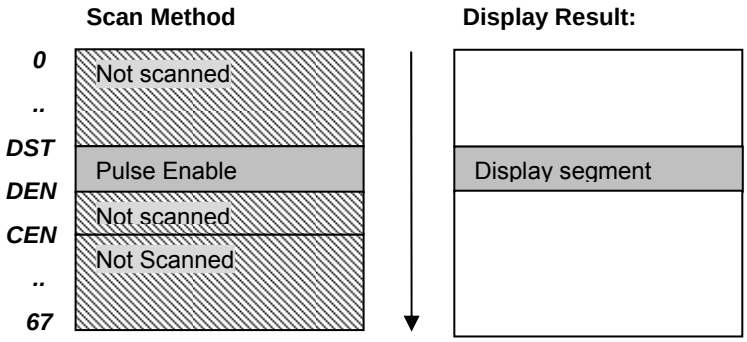
This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers. It's required to keep CEN ⩾CIC.

When LC[4]=1b, the Mux-Rate is narrowed down to DST-DEN+1. When MUX rate is reduced, reduce the frame rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be reduced.

For minimum power consumption, set LC[4]=1b, set (DST, DEN, CEN) to minimize Mux rate, use slowest frame rate which satisfies the flicker requirement, set PC[0]=0b, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement. When Mux-Rate is under 16, it is recommended to set BR=6 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



Serial Read Command (Enable only in S8/S9 mode):

25. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
			MX	MY	WA	DE	Prod_Code		**0**	Ver

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1603 via registers CEN, DST, DEN, and partial display control flag LC[3].

Combined with low power partial display mode and a low bias ratio of 6, UC1603 can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$BR = V_{LCD}/V_{BIAS}$,

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$, etc.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

UC1603 supports four bias ratios (BR) as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	6	7	8	**9**

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{o}C	**0.00**	- 0.05	- 0.10	- 0.15

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[1]. For good product reliability, it is recommended to keep V_{LCD} under 11.5 V for all temperature conditions.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by four control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two design constants. The values are provided in the Figure on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

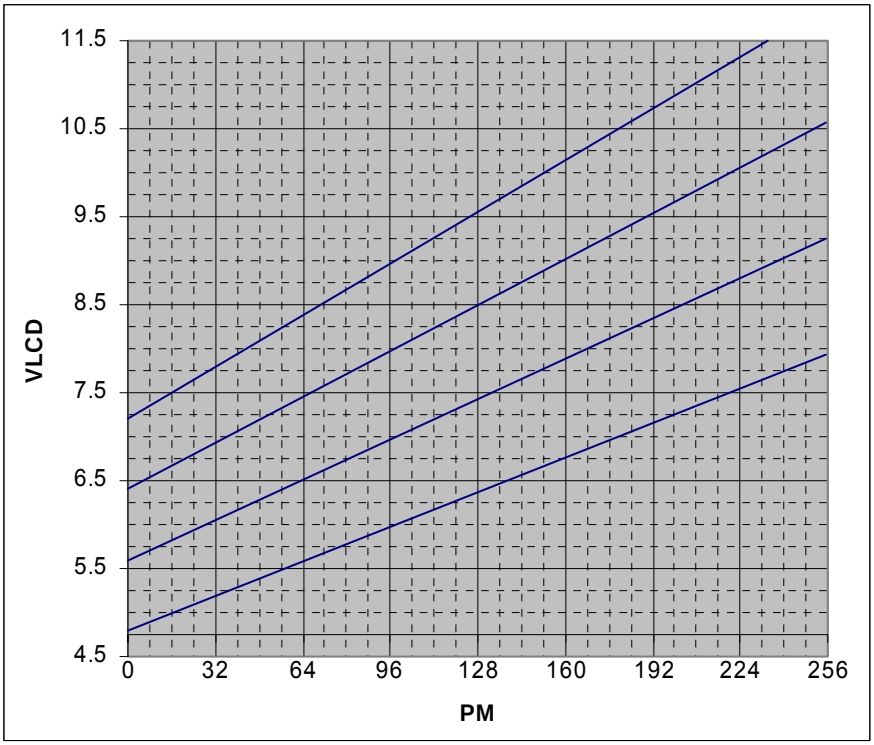
Black-and-white STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best result, software based approach for V_{LCD} adjustment is the recommended method for V_{LCD} fine-tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1603 designed to handle LCD panels with loading up to ~20nF using 20-Ω/Sq ITO glass with $V_{DD2/3} \geqslant 2.7V$. For larger LCD panels use lower resistance ITO glass packaging.

V_{LCD} QUICK REFERENCE



V_{LCD} Programming Curve.

BR	C_{V0} (V)	C_{PM} (mV)	PM	V_{LCD} Range (V)
6	4.800	12.24	0	4.80
			255	7.92
7	5.600	14.28	0	5.60
			255	9.24
8	6.400	16.32	0	6.40
			255	10.56
9	7.200	18.36	0	7.20
			234	11.50

Note:

1. For good product reliability, keep $V_{LCD\ (max)}$ under **11.5V** under all operating temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR REFERENCE CIRCUIT

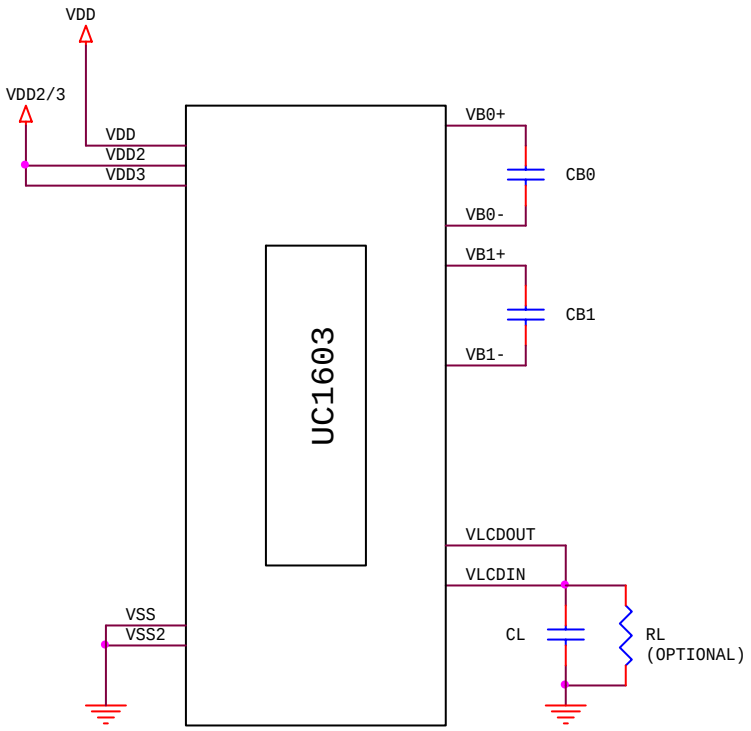


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

- Recommended component values:
  C_B: 150x~250x LCD load capacitance or 2.2uF (5V), whichever is higher.
  C_L: 330nF (25V) is appropriate for most applications.
  R_L: 3.3M~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1603 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Two different frame rates are provided for system design flexibility: 80 fps and 100fps.

Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG and COM drivers are in idle mode, their outputs are connected to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: COM*x* (where x = 1~68) refers to the row driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display ON* command. When DC[2] is set to OFF (logic “0”), both column and row drivers will become idle and UC1603 will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”,and UC1603 will first exit from Sleep Mode, restore the power (V_{LCD}, V_{BIAS} etc.) and then turn on row drivers and proper column drivers.

ALL PIXELS ON (APO)

When set, this flag will force all active column drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag set to ON, active column drivers will output the inverse of the value it received from the display buffer RAM. This flag has no impact on data stored in RAM.

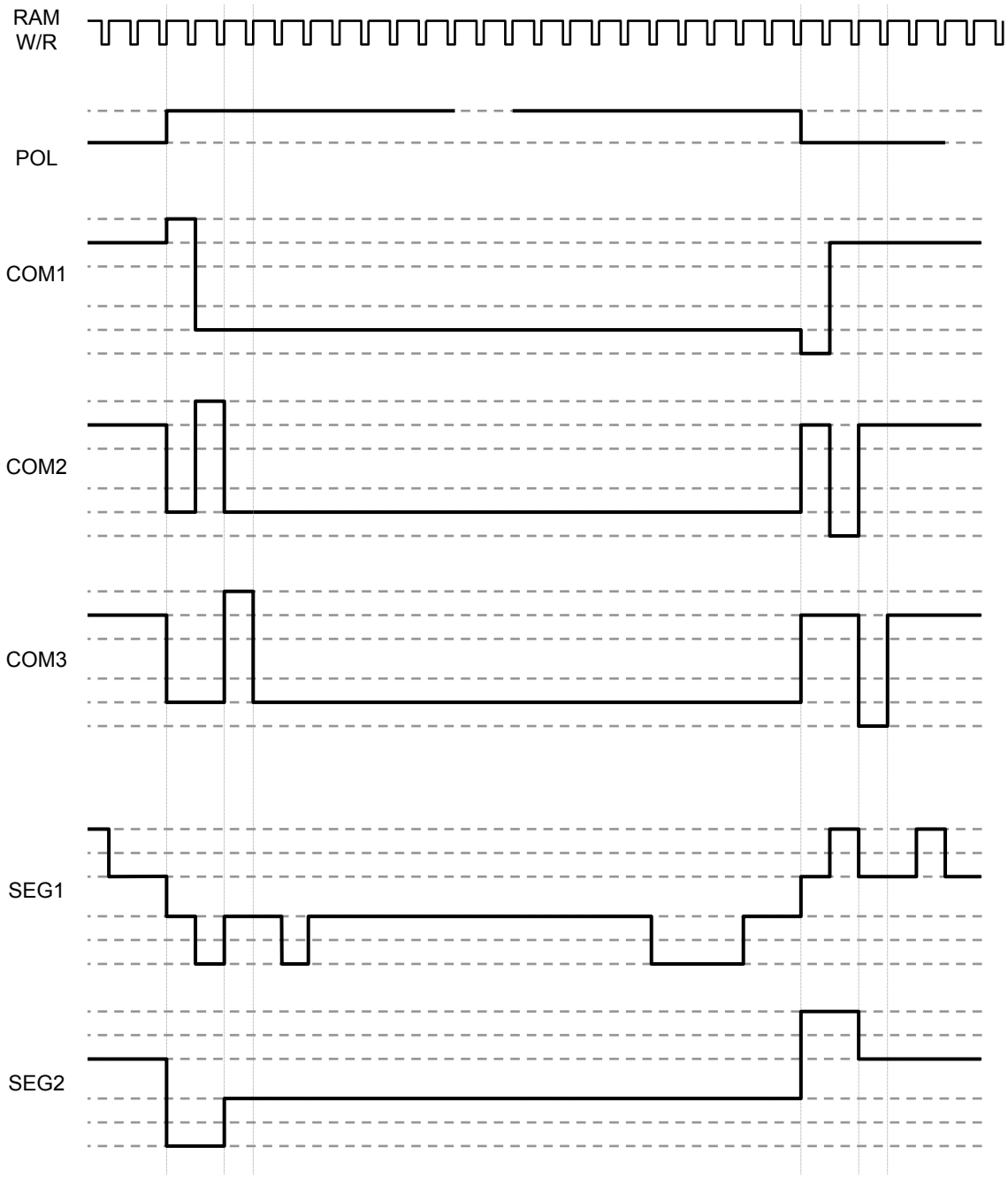


FIGURE 2: COM and SEG Electrode Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1603 supports 2 parallel and 3 serial bus protocols, which designers can use to create compact LCD modules.

		Bus Type				
		8080	**6800**	**S8 (4-wire)**	**S9 (3-wire)**	**I^2C (2-wire)**
Width		Parallel 8-bit		Serial		
Access		Read / Write				
Control & Data Pins	BM[1:0]	10	11	00	01	01
	DB[7]	Data		0	0	1
	CS[1:0]	Chip Select				A[3:2]
	CD	Control / Data			0	
	WR0	Write	R / W	0		
	WR1	Read	EN	0		
	DB[1,2,4~7]	Data		--		
	DB[3,0]	Data		DB[0]=SCK, DB[3]=SDA		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}.

	CS Disable Interface	CS Init bus state	RESET Init bus state
8-bit	✓	–	✓
S8 or S9	✓	✓	✓
I^2C	–	–	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- CS / RESET can be used to initialize bus state machine (like 8-bit / S8 / S9).
- RESET can be pin reset / soft reset / power on reset.

Table 3: Host Interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1603 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The read interface of Display RAM is implemented as a two-stage pipe-line. This architecture requires that every time memory address is modified by either `Set CA` or `Set PA` command, a dummy read cycle needs to be performed before the actual data can propagate through the pipe-line and be read from data port D.

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

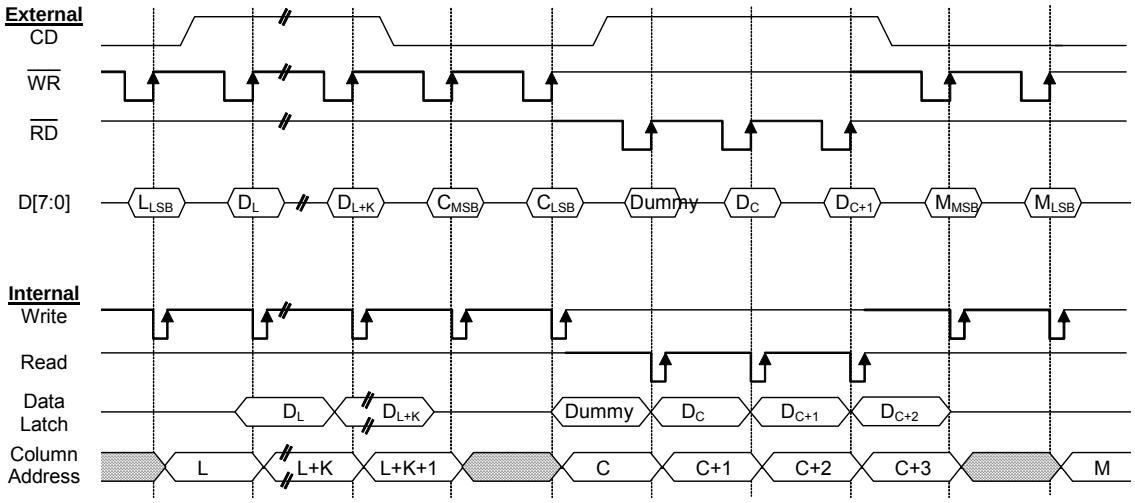


FIGURE 3: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1603 supports 3 serial modes, a 4-wire SPI mode (S8) and a 3-wire SPI mode (S9), and a 2-wire SPI (I^2C) mode. Bus interface mode is determined by the wiring of the BM. See table in last page for more detail.

S8 (4-wire) Interface

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

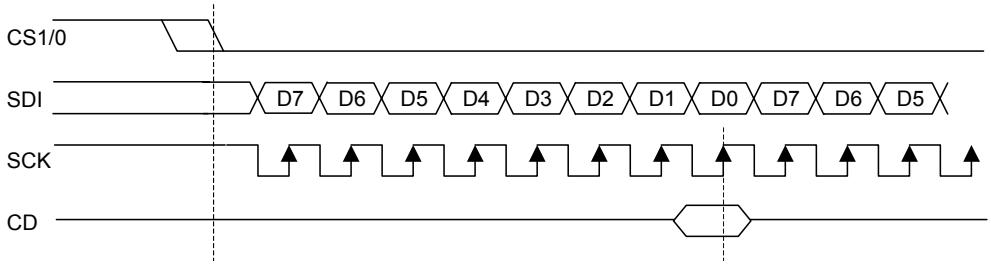


Figure 4.a: 4-wire Serial Interface (S8)

S9 (3-WIRE) INTERFACE

Only write operations are supported in this 3-wire serial mode. Pins CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

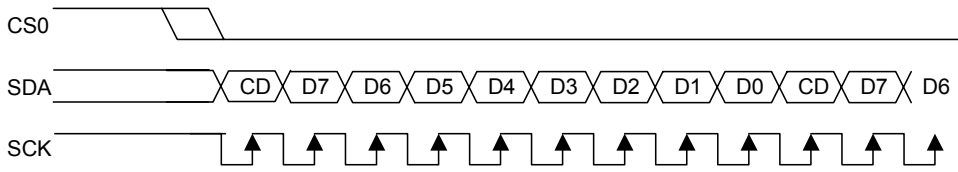


FIGURE 4.b: 3-wire Serial Interface (S9)

2-WIRE SERIAL INTERFACE (I^2C)

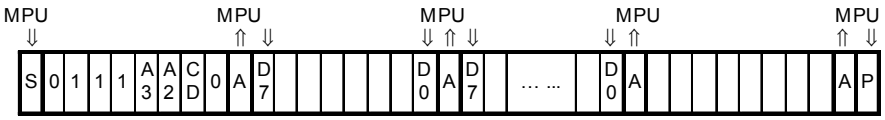
When BM[1:0] is set to "LH" and D[7:6] is set to "HH", UC1603 is configured as an I^2C bus signaling protocol compliant slave device. Please refer to I^2C standard for details of the bus signaling protocol, and the *AC Characteristics* section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and are used to configure UC1603's device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I^2C mode.

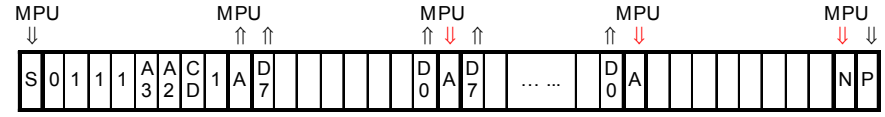
Each UC1603 I^2C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I^2C mode and should be connected to V_{SS}.

Write Mode



Read Mode

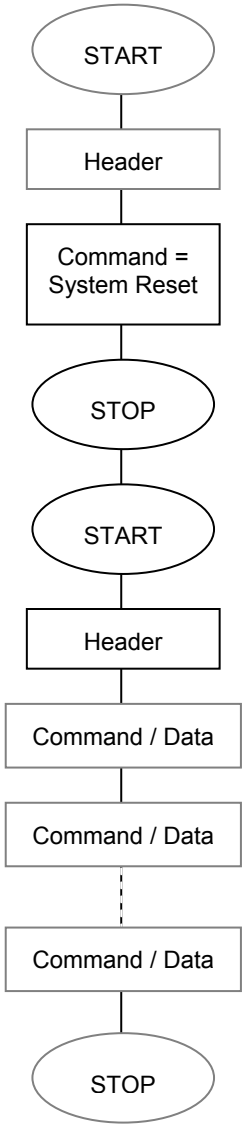


The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1603 will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1603) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the bus master.

When using I^2C serial mode, if command `System Reset` is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a “System Reset” command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



HOST INTERFACE REFERENCE CIRCUIT

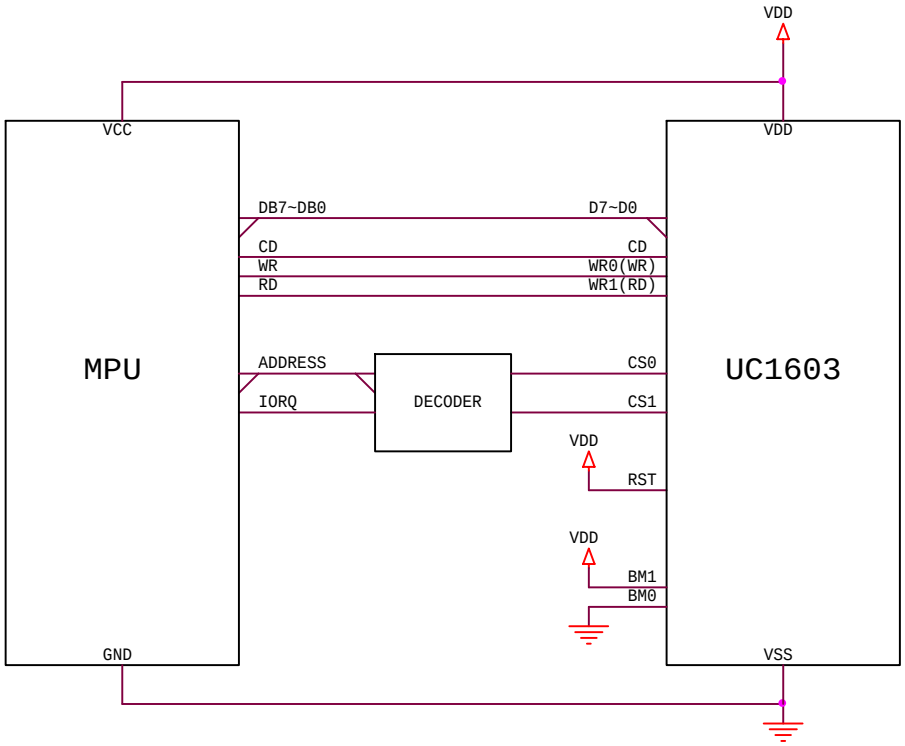


FIGURE 5: 8080/8-bit parallel mode example

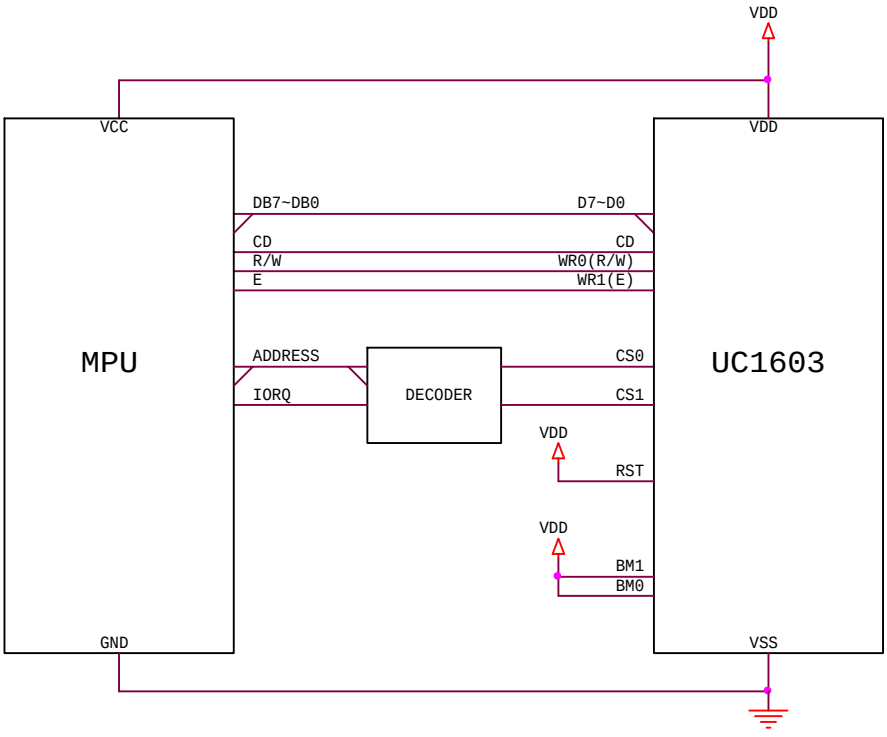


FIGURE 6: 6800/8-bit parallel mode example

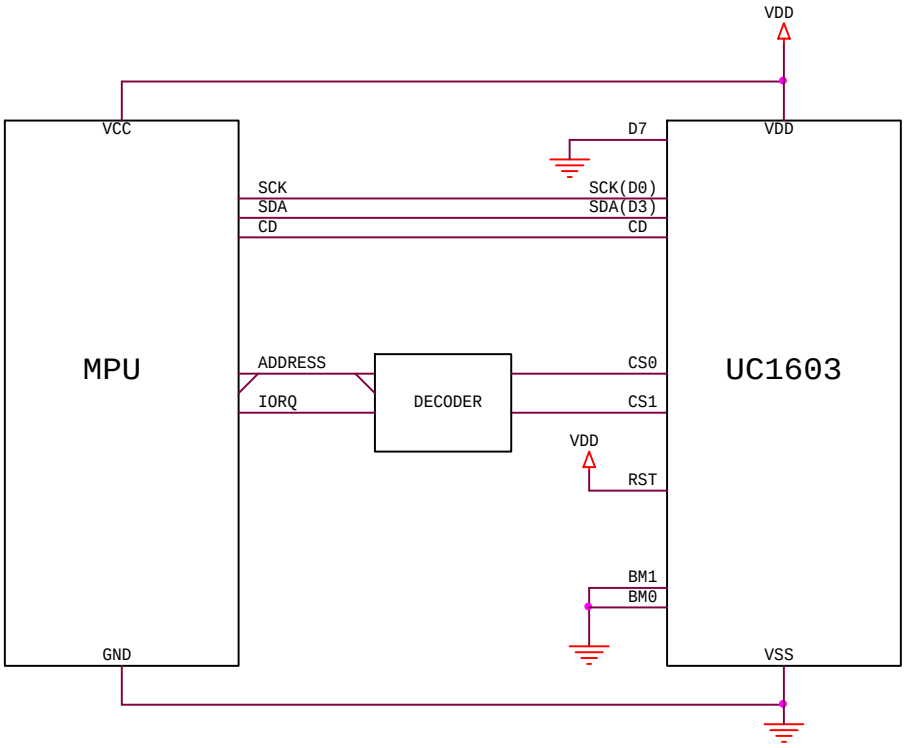


FIGURE 7: 4-wire SPI (S8) serial mode reference circuit

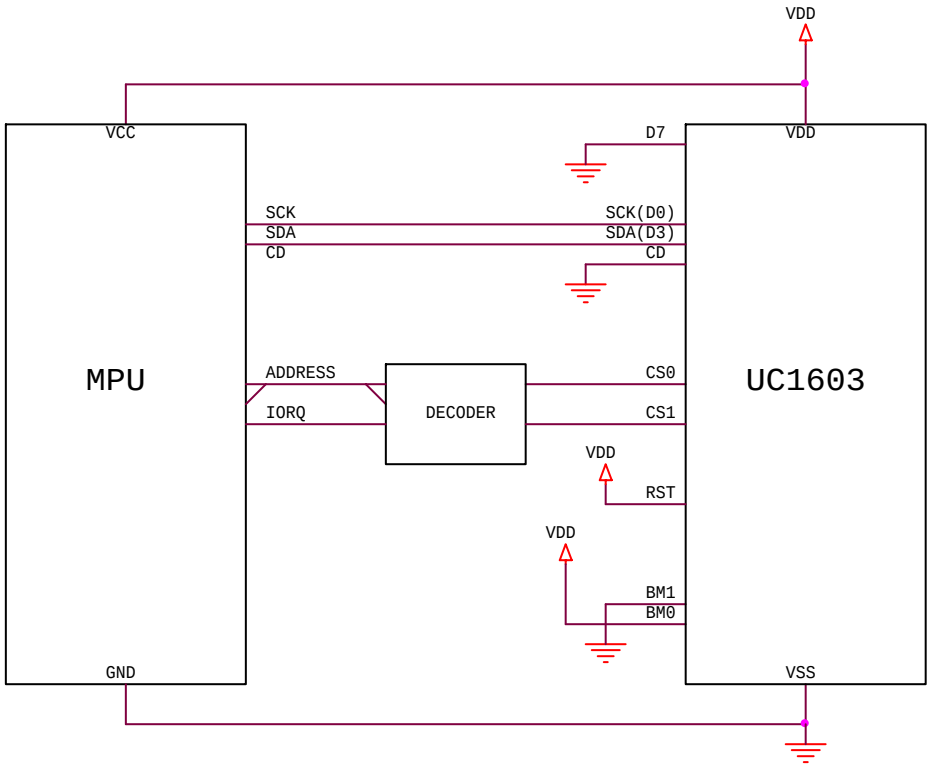


FIGURE 8: 3-wire SPI (S9) serial mode reference circuit

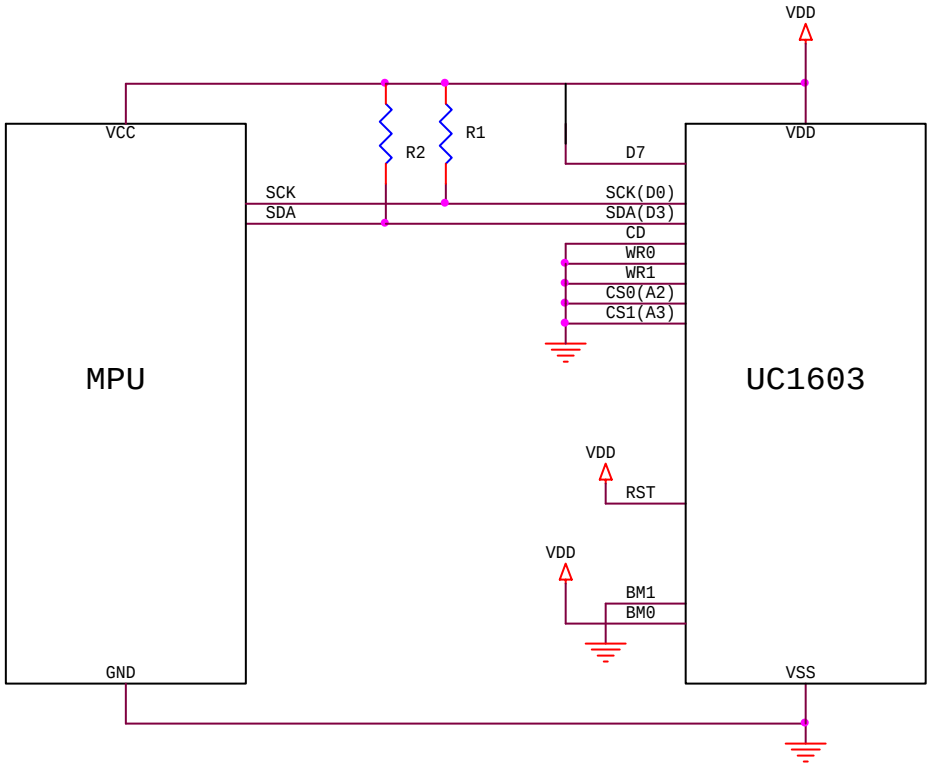


FIGURE 9: I^2C serial mode reference circuit

Note:

- RST pin is optional. When the RST pin is not used, connect it to V_{DD}.
- When using I^2C serial mode, CS1/0 are user configurable and affect A[3:2] of device address.
- R1, R2: 2k ~ 10k Ω, Use lower resistor for bus speed up to 3.6MHz; while use higher resistor for lower power.

DISPLAY DATA RAM (DDRAM)

DATA ORGANIZATION

The input display data is stored to a dual port static DDRAM (DDRAM, for Display Data RAM) organized as 68x98.

After setting CA and RA, the subsequent data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page among the relations of COM, SEG, SRAM, and various memory control registers.

DDRAM ACCESS

The DDRAM is a special purpose dual port RAM, which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DDRAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (97), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 7), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (97 – CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW SCANNING

For each field, the scanning starts at R1 through R*m*, where *m* depends on the setting of MR.

Row electrode scanning orders are not affected by Start Line (SL), or Mirror Y (MY, LC[1]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed R*m* scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*+1, 67)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produce the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches *67*.

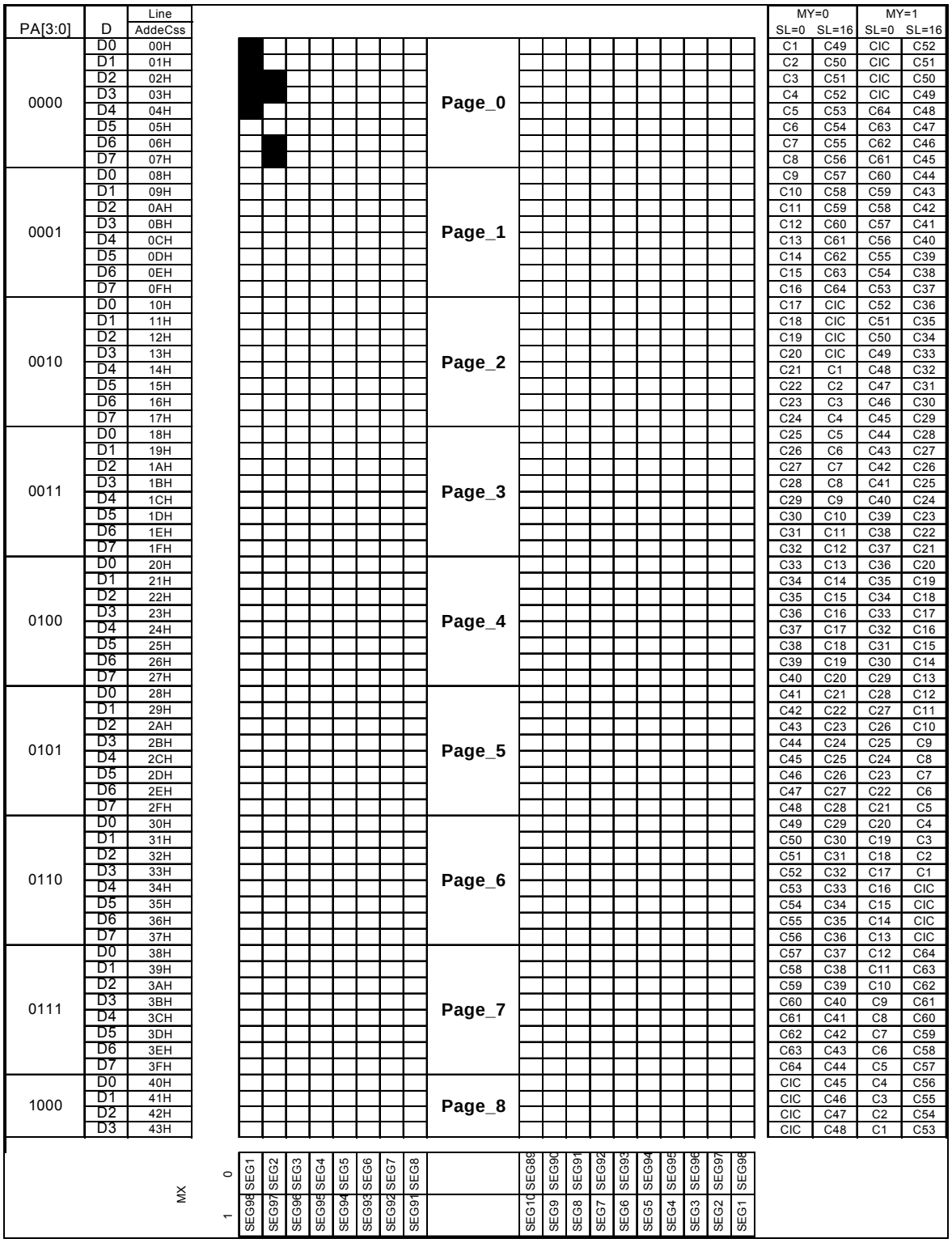
MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MR -1*, *67*)

Otherwise
Line = Mod(*Line-1* , *67*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.



PA[3:0]	D	Line AddeCss	Page	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
0000	D0	00H	Page_0	C1	C49	CIC	C52
	D1	01H		C2	C50	CIC	C51
	D2	02H		C3	C51	CIC	C50
	D3	03H		C4	C52	CIC	C49
	D4	04H		C5	C53	C64	C48
	D5	05H		C6	C54	C63	C47
	D6	06H		C7	C55	C62	C46
	D7	07H		C8	C56	C61	C45
0001	D0	08H	Page_1	C9	C57	C60	C44
	D1	09H		C10	C58	C59	C43
	D2	0AH		C11	C59	C58	C42
	D3	0BH		C12	C60	C57	C41
	D4	0CH		C13	C61	C56	C40
	D5	0DH		C14	C62	C55	C39
	D6	0EH		C15	C63	C54	C38
	D7	0FH		C16	C64	C53	C37
0010	D0	10H	Page_2	C17	CIC	C52	C36
	D1	11H		C18	CIC	C51	C35
	D2	12H		C19	CIC	C50	C34
	D3	13H		C20	CIC	C49	C33
	D4	14H		C21	C1	C48	C32
	D5	15H		C22	C2	C47	C31
	D6	16H		C23	C3	C46	C30
	D7	17H		C24	C4	C45	C29
0011	D0	18H	Page_3	C25	C5	C44	C28
	D1	19H		C26	C6	C43	C27
	D2	1AH		C27	C7	C42	C26
	D3	1BH		C28	C8	C41	C25
	D4	1CH		C29	C9	C40	C24
	D5	1DH		C30	C10	C39	C23
	D6	1EH		C31	C11	C38	C22
	D7	1FH		C32	C12	C37	C21
0100	D0	20H	Page_4	C33	C13	C36	C20
	D1	21H		C34	C14	C35	C19
	D2	22H		C35	C15	C34	C18
	D3	23H		C36	C16	C33	C17
	D4	24H		C37	C17	C32	C16
	D5	25H		C38	C18	C31	C15
	D6	26H		C39	C19	C30	C14
	D7	27H		C40	C20	C29	C13
0101	D0	28H	Page_5	C41	C21	C28	C12
	D1	29H		C42	C22	C27	C11
	D2	2AH		C43	C23	C26	C10
	D3	2BH		C44	C24	C25	C9
	D4	2CH		C45	C25	C24	C8
	D5	2DH		C46	C26	C23	C7
	D6	2EH		C47	C27	C22	C6
	D7	2FH		C48	C28	C21	C5
0110	D0	30H	Page_6	C49	C29	C20	C4
	D1	31H		C50	C30	C19	C3
	D2	32H		C51	C31	C18	C2
	D3	33H		C52	C32	C17	C1
	D4	34H		C53	C33	C16	CIC
	D5	35H		C54	C34	C15	CIC
	D6	36H		C55	C35	C14	CIC
	D7	37H		C56	C36	C13	CIC
0111	D0	38H	Page_7	C57	C37	C12	C64
	D1	39H		C58	C38	C11	C63
	D2	3AH		C59	C39	C10	C62
	D3	3BH		C60	C40	C9	C61
	D4	3CH		C61	C41	C8	C60
	D5	3DH		C62	C42	C7	C59
	D6	3EH		C63	C43	C6	C58
	D7	3FH		C64	C44	C5	C57
1000	D0	40H	Page_8	CIC	C45	C4	C56
	D1	41H		CIC	C46	C3	C55
	D2	42H		CIC	C47	C2	C54
	D3	43H		CIC	C48	C1	C53

Example for memory mapping: let MX = 0, MY = 0, SL = 0, according to the data shown in the above table:

⇒ Page0 SEG 1 (D7-D0) : 11100000b

⇒ Page0 SEG 2 (D7-D0) : 00110011b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1603 has two different types of Reset:

Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1603 enters RESET sequence:

- Operation mode will be “Reset”
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1603 has three operating modes (OM):
Reset, Sleep, Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-On-Reset, two commands will initiate OM transitions:
Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0}, C_{B1}, and C_L. To drain these capacitors, use Reset command to activate the on-chip draining circuit.

Action	Mode	OM
Reset command RST_ pin pulled “L” Power ON reset	Reset	00
Set Driver Enable to “0”	Sleep	10
Set Driver Enable to “1”	Normal	11

Table 5: OM changes

Even though UC1603 consumes very little energy in Sleep mode (typically 2μA or less); however, since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1603 contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing row and column drivers from their OFF states. When exiting Sleep Mode and Reset Mode, column and row drivers will not be activated until UC1603 internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1603 power-up sequence is simplified by built-in "Power Ready" flags and by the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 5~10 mS before CPU starting to issue commands to UC1603. No additional time sequences are required for enabling of the charge pump, turning on the display drivers and writing to RAM or any other commands.

There's no delay needed while turning on V_{DD} and $V_{DD2/3}$, and either one can be turned on first.

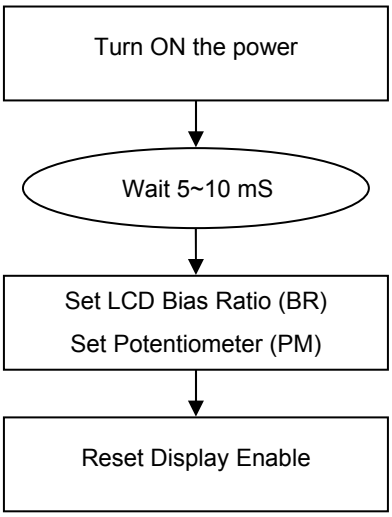


FIGURE 10: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX}, and C_{LCD} from damaging the LCD when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

The draining resistance is 3K Ω for both V_{LCD} and V_B. It is recommended to wait *3* x *RC* for V_{LCD} and *1.5 x RC* for V_B. For example, if C_{LCD} is 330nF, then the draining time required for V_{LCD} is 0.5~1mS.

When internal V_{LCD} is not used, UC1603 will *not* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

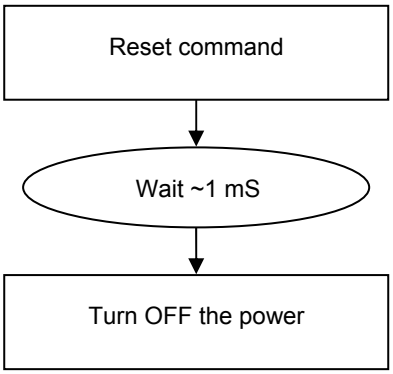


FIGURE 11: Reference Power-Down Sequence

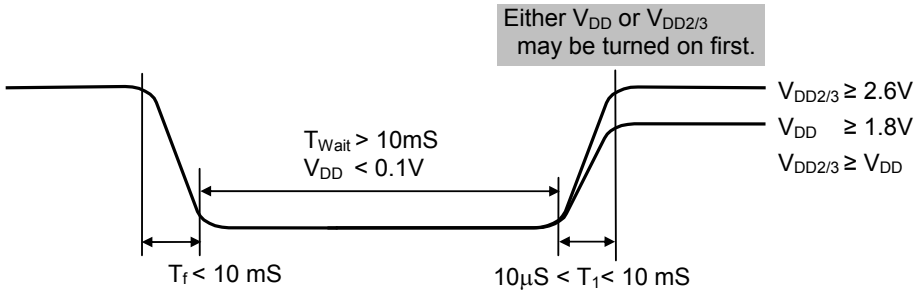


Figure 12: Power Off-On Sequence

SAMPLE COMMAND SEQUENCES FOR POWER MANAGEMENT

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)
Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~5mS after V_{DD} is ON
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping Control	
A	0	0	1	0	1	0	0	0	0	#	Set Frame Rate	Fine tune for power, flicker, contrast.
C	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is, therefore, highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1603 require special "ESD Sensitivity" consideration in particular:

TEST MODE / Pins		MM *		HBM *	
		V_{DD}	V_{SS}	V_{DD}	V_{SS}
LCD Driver		200V	200V	2.5K	2.0K
LCM Digital Interface		300V	300V	3.0K	3.0K
LCM HV Interface	TST1/2/4	200V	200V	3.0K	3.0K
	C_B pins	300V	300V	3.0K	3.0K
	V_{LCDIN}	300V	300V	3.0K	3.0K
	V_{LCDOUT}	300V	300V	3.0K	3.0K
PWR/GND		--	300V	--	3.0K

* MM: Machine Mode; HBM: Human Body Mode

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134 – notes 1 and 2.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Generated voltage	-0.3	+13.2	V
V_{IN} / V_{OUT}	Any input/output	-0.4	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Notes

1. V_{DD} is based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.465	V
$V_{DD2/3}$	Supply for bias & pump		2.5		3.465	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant 2.6V$, 25°C			11.5	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant 2.6V$, 25°C	0.80		1.32	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
I_{SB}	Standby current	$V_{DD} = V_{DD2/3} = 3.3V$, Temp = 85°C			50	μA
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 11V		2	3	kΩ
$R_{0(COM)}$	COM output impedance	V_{LCD} = 11V		2	3	kΩ
F_{FR}	Average Frame Rate	LC[2] = 0b	-10%	80	+10%	Hz

Note : Voltages exceeding the Max. value may still keep the IC operating properly, yet might shorten its lifetime.

POWER CONSUMPTION

V_{DD} = 2.7 V,
V_{LCD} = 10.01 V
Mux Rate = 68,
C_B = 2.2 μF

Bias Ratio = 9,
Frame Rate = 0b,
Bus mode = 6800,
Temperature = 25°C,

PM = 153,
Panel Loading (PC[0]) ⩽ 12nF,
C_L = 330 nF,
All outputs are open circuit.

Display Pattern	Conditions	Typ. (μA)	Max. (μA)
All-OFF	Bus = idle	189	(TBD)
2-pixel checker	Bus = idle	195	(TBD)
--	Bus = idle (standby current)	--	5

AC CHARACTERISTICS

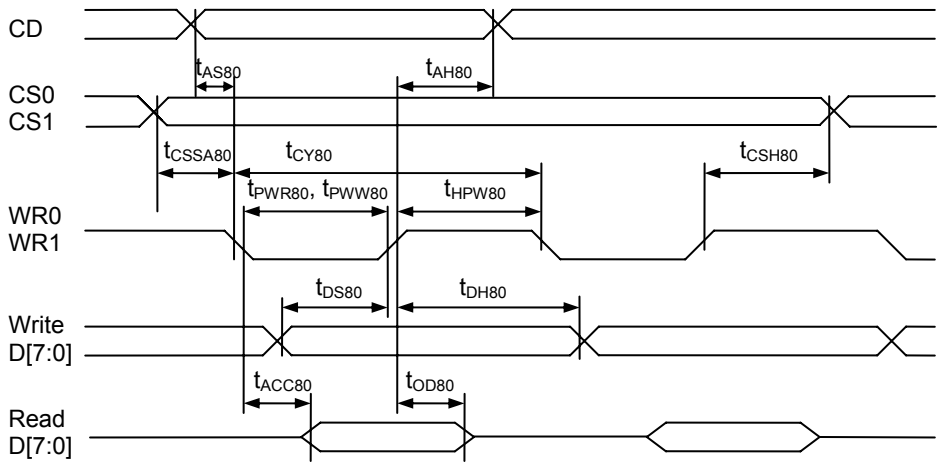


FIGURE 13: Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address	setup time hold time		0 0	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select	setup time hold time		5 5	–	nS
t_{CY80}		Cycle time	read write		120 80	–	nS
t_{PWR80} t_{PWW80}	WR1 WR0	Pulse width	read write		60 40	–	nS
t_{HPW80}	WR0, WR1	High pulse width	read write		60 40	–	nS
t_{DS80} t_{DH80}	D0~D7	Data	setup time hold time		30 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time		C_L = 100pF	– 15	60 30	nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address	setup time hold time		0 0	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select	setup time hold time		5 5	–	nS
t_{CY80}		Cycle time	read write		240 160	–	nS
t_{PWR80} t_{PWW80}	WR1 WR0	Pulse width	read write		120 80	–	nS
t_{HPW80}	WR0, WR1	High pulse width	read write		120 80	–	nS
t_{DS80} t_{DH80}	D0~D7	Data	setup time hold time		60 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time		C_L = 100pF	– 15	60 30	nS

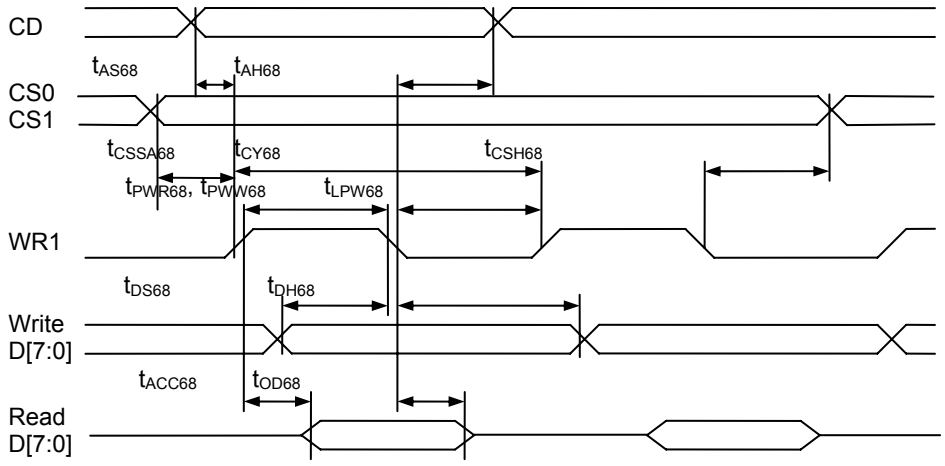


FIGURE 14: Parallel Bus Timing Characteristics (for 6800 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address	setup time hold time		0 0	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select	setup time hold time		5 5		nS
t_{CY68}		Cycle time	read write		120 80	–	nS
t_{PWR68} t_{PWW68}	WR1	Pulse width	read write		60 40	–	nS
t_{HPW68}		High pulse width	read write		60 40	–	nS
t_{DS68} t_{DH68}	D0~D7	Data	setup time hold time		30 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time		C_L = 100pF	– 15	60 30	nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address	setup time hold time		0 0	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select	setup time hold time		5 5		nS
t_{CY68}		Cycle time	read write		240 160	–	nS
t_{PWR68} t_{PWW68}	WR1	Pulse width	read write		120 80	–	nS
t_{HPW68}		High pulse width	read write		120 80	–	nS
t_{DS68} t_{DH68}	D0~D7	Data	setup time hold time		60 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time		C_L = 100pF	– 15	60 30	nS

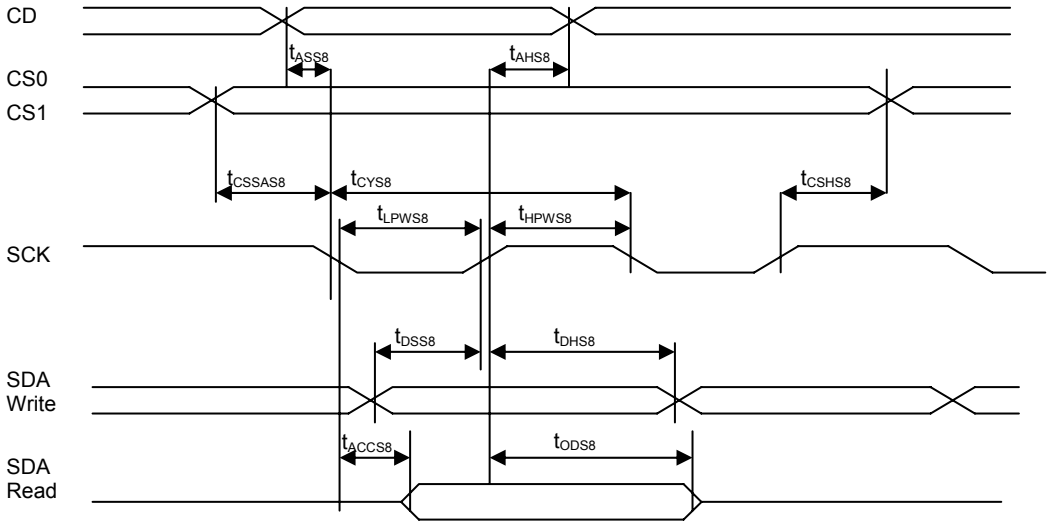


FIGURE 15: Serial Bus Timing Characteristics (for S8)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{ASS8} t_{AHS8}	CD	Address	setup time hold time		0 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select	setup time hold time		5 5		nS
t_{CYS8}	SCK	Cycle time	read write		40 30	–	nS
t_{LPWS8}		Low pulse width	read write		20 15	–	nS
t_{HPWS8}		High pulse width	read write		20 15	–	nS
t_{DSS8} t_{DHS8}	SDA	Data	setup time hold time		12 0	–	nS
t_{ACCS8} t_{ODS8}		Read access time Output disable time		C_L = 100pF	– N/A	15 N/A	nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{ASS8} t_{AHS8}	CD	Address	setup time hold time		0 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select	setup time hold time		10 10		nS
t_{CYS8}	SCK	Cycle time	read write		80 60	–	nS
t_{LPWS8}		Low pulse width	read write		40 30	–	nS
t_{HPWS8}		High pulse width	read write		40 30	–	nS
t_{DSS8} t_{DHS8}	SDA	Data	setup time hold time		24 0	–	nS
t_{ACCS8} t_{ODS8}		Read access time Output disable time		C_L = 100pF	– N/A	15 N/A	nS

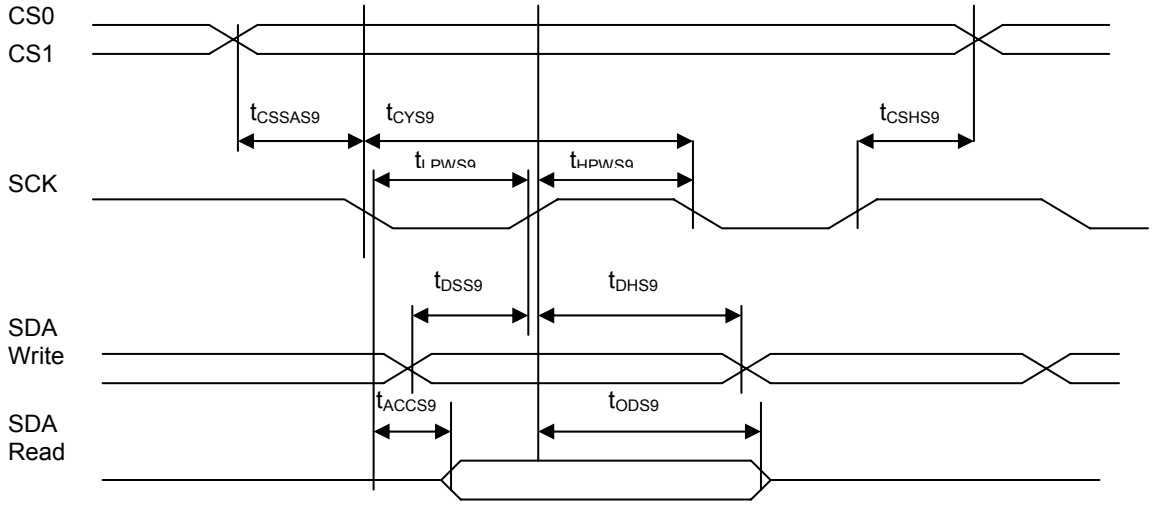


FIGURE 16: Serial Bus Timing Characteristics (for S9)

(2.5V ⩽ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select	setup time hold time		5 5		nS
t_{CYS9}	SCK	Cycle time	read write		40 30	–	nS
t_{LPWS9}		Low pulse width	read write		20 15	–	nS
t_{HPWS9}		High pulse width	read write		20 15	–	nS
t_{DSS9} t_{DHS9}	SDA	Data	setup time hold time		12 0	–	nS
t_{ACCS9} t_{ODS9}		Read access time Output disable time		C_L = 100pF	– N/A	15 N/A	nS

(1.65V ⩽ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select	setup time hold time		10 10		nS
t_{CYS9}	SCK	Cycle time	read write		80 60	–	nS
t_{LPWS9}		Low pulse width	read write		40 30	–	nS
t_{HPWS9}		High pulse width	read write		40 30	–	nS
t_{DSS9} t_{DHS9}	SDA	Data	setup time hold time		24 0	–	nS
t_{ACCS9} t_{ODS9}		Read access time Output disable time		C_L = 100pF	– N/A	15 N/A	nS

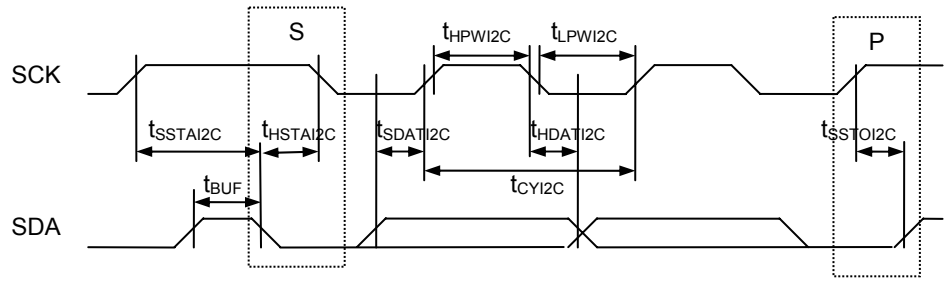


FIGURE 17: Serial bus timing characteristics (for I^2C)

(2.5V ⩽ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time	read	tr+tf ⩽ 100nS	580	–	nS
			write		275		
t_{LPWI2C}		Low pulse width	read		290	–	nS
			write		165		
t_{HPWI2C}		High pulse width	read		290	–	nS
			write		110		
tr, tf	SCK SDA	Rise time and fall time			–	–	nS
$t_{SSDAI2C}$		Data	setup time		28	–	nS
t_{HDAI2C}			hold time		11		
$t_{SSTAI2C}$		START	setup time		28	–	nS
$t_{HSTAI2C}$			hold time		50		
$t_{SSTOI2C}$		STOP	setup time		28	–	nS
t_{BUF}		Bus Free time between STOP and START condition			165	–	nS

(1.65V ⩽ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description		Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time	read	tr+tf ⩽ 100nS	750	–	nS
			write		330		
t_{LPWI2C}		Low pulse width	read		375	–	nS
			write		200		
t_{HPWI2C}		High pulse width	read		375	–	nS
			write		130		
tr, tf	SCK SDA	Rise time and fall time			–	–	nS
$t_{SSDAI2C}$		Data	setup time		55	–	nS
t_{HDAI2C}			hold time		11		
$t_{SSTAI2C}$		START	setup time		28	–	nS
$t_{HSTAI2C}$			hold time		60		
$t_{SSTOI2C}$		STOP	setup time		28	–	nS
t_{BUF}		Bus Free Time between STOP and START condition			220		nS

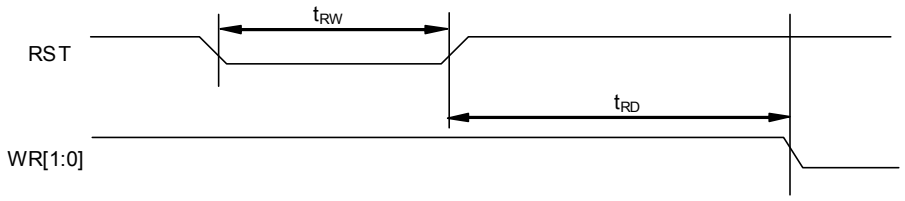


FIGURE 18: Reset Characteristics

(1.65V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1	–	μS
t_{RD}	RST, WR	Reset to WR pulse delay		10		mS

PHYSICAL DIMENSIONS

DIE SIZE:
4984 x 745 μM^2 ± 40 μM

DIE THICKNESS:
400 mm ± 20 mm

BUMP HEIGHT:
15 μM ± 3 mm
$H_{MAX} – H_{MIN}$ (within die) ≤ 2 μM

SEG / COM SIZE:
19.5 x 103 μM (Typ.)

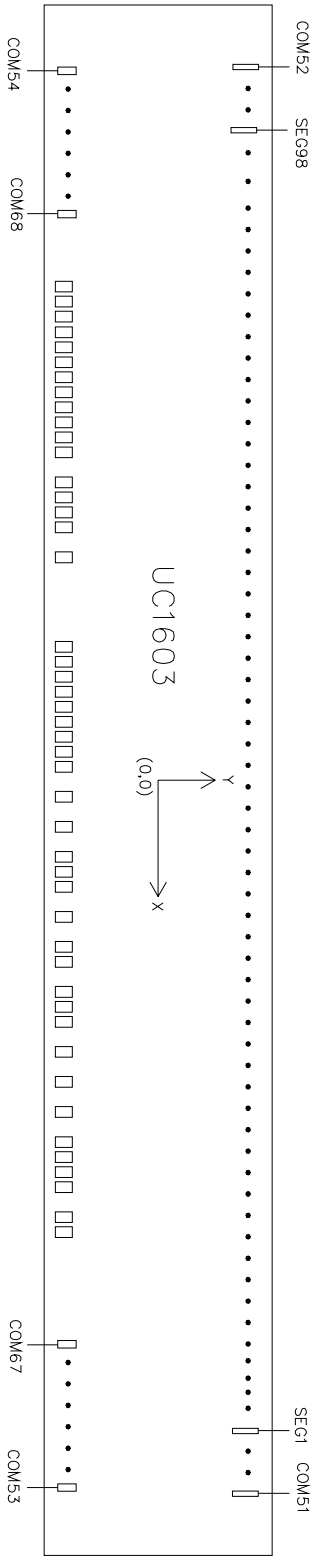
BUMP PITCH:
32.5 μM (Typ.)

BUMP GAP:
13 μM (Typ.)

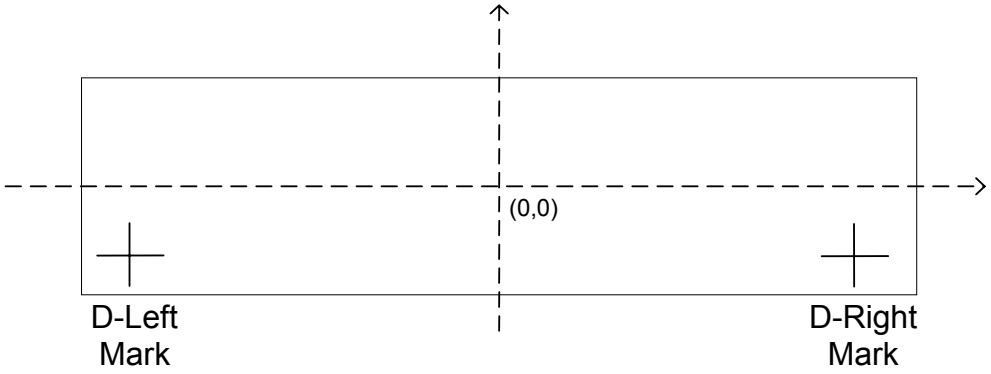
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

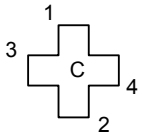
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

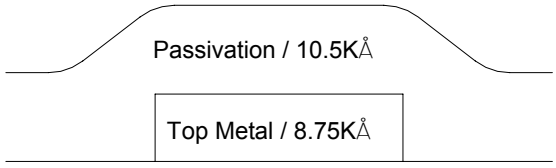
Alignment mark is on Metal3 under Passivation.

The "x" and "+" marks are symmetric both horizontally and vertically.

COORDINATES:

	D-Left Mark Center		D-Right Mark Center	
	X	Y	X	Y
1	-2112	-255	2092	-255
2	-2092	-330	2112	-330
3	-2139.5	-282.5	2064.5	-282.5
4	-2064.5	-302.5	2139.5	-302.5
C	-2102	-292.5	2102	-292.5

TOP METAL AND PASSIVATION:



FOR PROCESS CROSS-SECTION

PAD COORDINATES

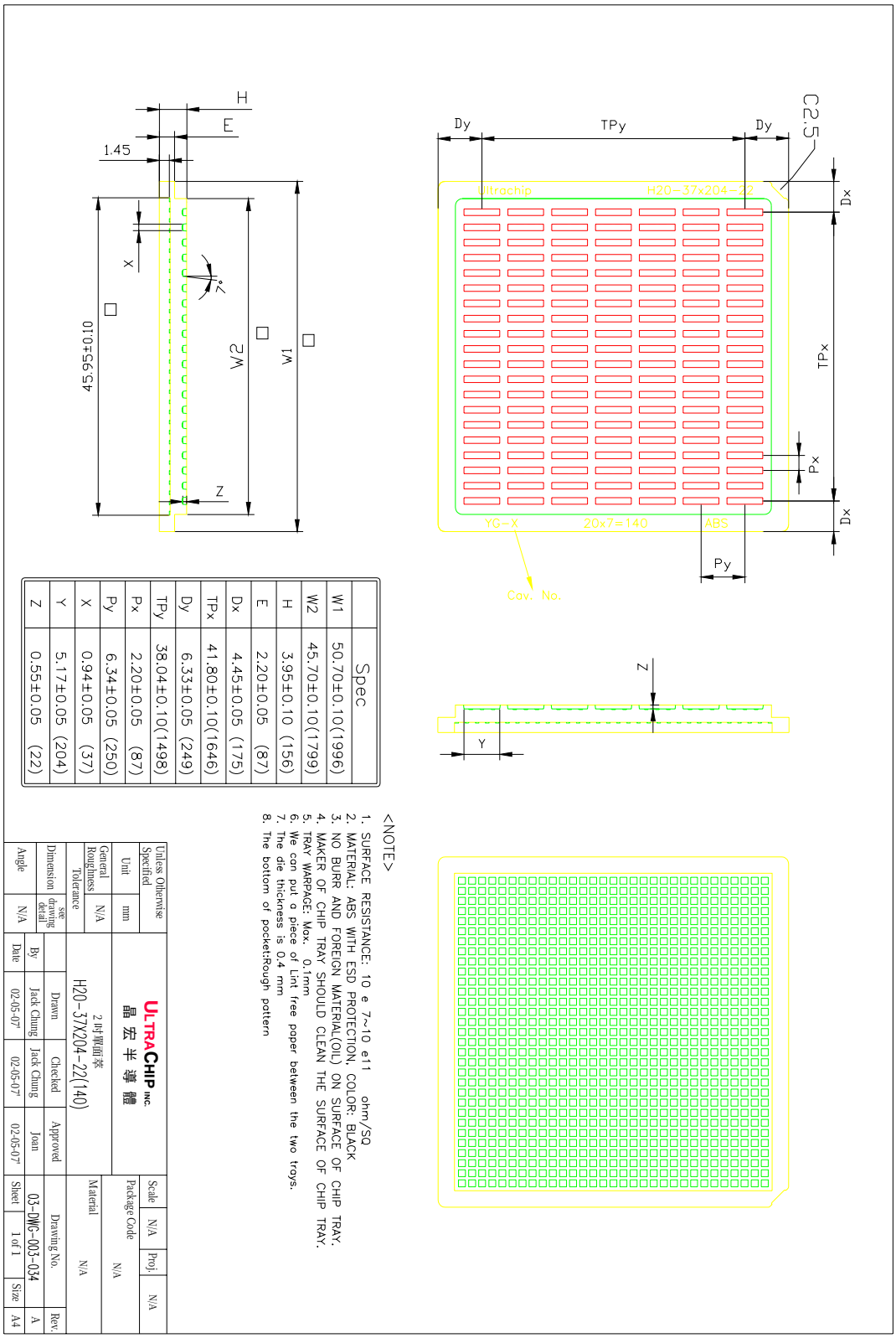
#	Pad	X	Y	W	H
1	COM54	-2421.25	-286.5	19.5	103
2	COM56	-2388.75	-286.5	19.5	103
3	COM58	-2356.25	-286.5	19.5	103
4	COM60	-2323.75	-286.5	19.5	103
5	COM62	-2291.25	-286.5	19.5	103
6	COM64	-2258.75	-286.5	19.5	103
7	COM66	-2226.25	-286.5	19.5	103
8	COM68	-2193.75	-286.5	19.5	103
9	CS0	-2002.4	-301.275	65	71.45
10	CS1	-1920.8	-301.275	65	71.45
11	RST	-1839.2	-301.275	65	71.45
12	CD	-1757.6	-301.275	65	71.45
13	DATA0	-1667.65	-301.275	65	71.45
14	DATA1	-1582.55	-301.275	65	71.45
15	DATA2	-1497.45	-301.275	65	71.45
16	DATA3	-1412.35	-301.275	65	71.45
17	DATA4	-1327.25	-301.275	65	71.45
18	DATA5	-1242.15	-301.275	65	71.45
19	DATA6	-1157.05	-301.275	65	71.45
20	DATA7	-1071.95	-301.275	65	71.45
21	WR0	-982	-301.275	65	71.45
22	WR1	-900.4	-301.275	65	71.45
23	vssx	-820.6	-301.275	45	71.45
24	vdd	-724.9	-301.275	45	71.45
25	vdd	-664.9	-301.275	45	71.45
26	vdd2	-604.9	-301.275	45	71.45
27	vdd2	-544.9	-301.275	45	71.45
28	vdd3	-303.5	-301.275	45	71.45
29	vdd3	-243.5	-301.275	45	71.45
30	vss	-183.5	-301.275	45	71.45
31	vss	-123.5	-301.275	45	71.45
32	vss	-63.5	-301.275	45	71.45
33	vss	-3.5	-301.275	45	71.45
34	vss2	56.7	-301.275	45	71.45
35	vss2	116.7	-301.275	45	71.45
36	vss2	176.7	-301.275	45	71.45
37	TST4	256.5	-301.275	65	71.45
38	TST2	358.3	-291	65	92
39	TST1	465.5	-291	65	92
40	VB1+	648.3	-291	65	92
41	VB1+	747.3	-291	65	92
42	BM0	843.1	-301.275	65	71.45
43	BM1	924.7	-301.275	65	71.45
44	VB1-	1020.5	-291	65	92
45	VB1-	1119.5	-291	65	92
46	vssx	1215.9	-291	65	92
47	VB0-	1312.3	-291	65	92
48	VB0-	1411.3	-291	65	92
49	VB0+	1491.3	-291	65	92
50	VB0+	1590.3	-291	65	92
51	VLCDOUT	1744.7	-291	65	92
52	VLCDOUT	1849.1	-291	65	92
53	VLCDIN	1949.1	-291	65	92
54	COM67	2193.75	-286.5	19.5	103
55	COM65	2226.25	-286.5	19.5	103
56	COM63	2258.75	-286.5	19.5	103
57	COM61	2291.25	-286.5	19.5	103
58	COM59	2323.75	-286.5	19.5	103
59	COM57	2356.25	-286.5	19.5	103
60	COM55	2388.75	-286.5	19.5	103
61	COM53	2421.25	-286.5	19.5	103
62	COM51	2421.25	286.5	19.5	103

#	Pad	X	Y	W	H
63	COM49	2388.75	286.5	19.5	103
64	COM47	2356.25	286.5	19.5	103
65	COM45	2323.75	286.5	19.5	103
66	COM43	2291.25	286.5	19.5	103
67	COM41	2258.75	286.5	19.5	103
68	COM39	2226.25	286.5	19.5	103
69	COM37	2193.75	286.5	19.5	103
70	COM35	2161.25	286.5	19.5	103
71	COM33	2128.75	286.5	19.5	103
72	COM31	2096.25	286.5	19.5	103
73	COM29	2063.75	286.5	19.5	103
74	COM27	2031.25	286.5	19.5	103
75	COM25	1998.75	286.5	19.5	103
76	COM23	1966.25	286.5	19.5	103
77	COM21	1933.75	286.5	19.5	103
78	COM19	1901.25	286.5	19.5	103
79	COM17	1868.75	286.5	19.5	103
80	COM15	1836.25	286.5	19.5	103
81	COM13	1803.75	286.5	19.5	103
82	COM11	1771.25	286.5	19.5	103
83	COM9	1738.75	286.5	19.5	103
84	COM7	1706.25	286.5	19.5	103
85	COM5	1673.75	286.5	19.5	103
86	COM3	1641.25	286.5	19.5	103
87	COM1	1608.75	286.5	19.5	103
88	SEG1	1576.25	286.5	19.5	103
89	SEG2	1543.75	286.5	19.5	103
90	SEG3	1511.25	286.5	19.5	103
91	SEG4	1478.75	286.5	19.5	103
92	SEG5	1446.25	286.5	19.5	103
93	SEG6	1413.75	286.5	19.5	103
94	SEG7	1381.25	286.5	19.5	103
95	SEG8	1348.75	286.5	19.5	103
96	SEG9	1316.25	286.5	19.5	103
97	SEG10	1283.75	286.5	19.5	103
98	SEG11	1251.25	286.5	19.5	103
99	SEG12	1218.75	286.5	19.5	103
100	SEG13	1186.25	286.5	19.5	103
101	SEG14	1153.75	286.5	19.5	103
102	SEG15	1121.25	286.5	19.5	103
103	SEG16	1088.75	286.5	19.5	103
104	SEG17	1056.25	286.5	19.5	103
105	SEG18	1023.75	286.5	19.5	103
106	SEG19	991.25	286.5	19.5	103
107	SEG20	958.75	286.5	19.5	103
108	SEG21	926.25	286.5	19.5	103
109	SEG22	893.75	286.5	19.5	103
110	SEG23	861.25	286.5	19.5	103
111	SEG24	828.75	286.5	19.5	103
112	SEG25	796.25	286.5	19.5	103
113	SEG26	763.75	286.5	19.5	103
114	SEG27	731.25	286.5	19.5	103
115	SEG28	698.75	286.5	19.5	103
116	SEG29	666.25	286.5	19.5	103
117	SEG30	633.75	286.5	19.5	103
118	SEG31	601.25	286.5	19.5	103
119	SEG32	568.75	286.5	19.5	103
120	SEG33	536.25	286.5	19.5	103
121	SEG34	503.75	286.5	19.5	103
122	SEG35	471.25	286.5	19.5	103
123	SEG36	438.75	286.5	19.5	103
124	SEG37	406.25	286.5	19.5	103

#	Pad	X	Y	W	H
125	SEG38	373.75	286.5	19.5	103
126	SEG39	341.25	286.5	19.5	103
127	SEG40	308.75	286.5	19.5	103
128	SEG41	276.25	286.5	19.5	103
129	SEG42	243.75	286.5	19.5	103
130	SEG43	211.25	286.5	19.5	103
131	SEG44	178.75	286.5	19.5	103
132	SEG45	146.25	286.5	19.5	103
133	SEG46	113.75	286.5	19.5	103
134	SEG47	81.25	286.5	19.5	103
135	SEG48	48.75	286.5	19.5	103
136	SEG49	16.25	286.5	19.5	103
137	SEG50	-16.25	286.5	19.5	103
138	SEG51	-48.75	286.5	19.5	103
139	SEG52	-81.25	286.5	19.5	103
140	SEG53	-113.75	286.5	19.5	103
141	SEG54	-146.25	286.5	19.5	103
142	SEG55	-178.75	286.5	19.5	103
143	SEG56	-211.25	286.5	19.5	103
144	SEG57	-243.75	286.5	19.5	103
145	SEG58	-276.25	286.5	19.5	103
146	SEG59	-308.75	286.5	19.5	103
147	SEG60	-341.25	286.5	19.5	103
148	SEG61	-373.75	286.5	19.5	103
149	SEG62	-406.25	286.5	19.5	103
150	SEG63	-438.75	286.5	19.5	103
151	SEG64	-471.25	286.5	19.5	103
152	SEG65	-503.75	286.5	19.5	103
153	SEG66	-536.25	286.5	19.5	103
154	SEG67	-568.75	286.5	19.5	103
155	SEG68	-601.25	286.5	19.5	103
156	SEG69	-633.75	286.5	19.5	103
157	SEG70	-666.25	286.5	19.5	103
158	SEG71	-698.75	286.5	19.5	103
159	SEG72	-731.25	286.5	19.5	103
160	SEG73	-763.75	286.5	19.5	103
161	SEG74	-796.25	286.5	19.5	103
162	SEG75	-828.75	286.5	19.5	103
163	SEG76	-861.25	286.5	19.5	103
164	SEG77	-893.75	286.5	19.5	103
165	SEG78	-926.25	286.5	19.5	103
166	SEG79	-958.75	286.5	19.5	103
167	SEG80	-991.25	286.5	19.5	103
168	SEG81	-1023.75	286.5	19.5	103

#	Pad	X	Y	W	H
169	SEG82	-1056.25	286.5	19.5	103
170	SEG83	-1088.75	286.5	19.5	103
171	SEG84	-1121.25	286.5	19.5	103
172	SEG85	-1153.75	286.5	19.5	103
173	SEG86	-1186.25	286.5	19.5	103
174	SEG87	-1218.75	286.5	19.5	103
175	SEG88	-1251.25	286.5	19.5	103
176	SEG89	-1283.75	286.5	19.5	103
177	SEG90	-1316.25	286.5	19.5	103
178	SEG91	-1348.75	286.5	19.5	103
179	SEG92	-1381.25	286.5	19.5	103
180	SEG93	-1413.75	286.5	19.5	103
181	SEG94	-1446.25	286.5	19.5	103
182	SEG95	-1478.75	286.5	19.5	103
183	SEG96	-1511.25	286.5	19.5	103
184	SEG97	-1543.75	286.5	19.5	103
185	SEG98	-1576.25	286.5	19.5	103
186	COM2	-1608.75	286.5	19.5	103
187	COM4	-1641.25	286.5	19.5	103
188	COM6	-1673.75	286.5	19.5	103
189	COM8	-1706.25	286.5	19.5	103
190	COM10	-1738.75	286.5	19.5	103
191	COM12	-1771.25	286.5	19.5	103
192	COM14	-1803.75	286.5	19.5	103
193	COM16	-1836.25	286.5	19.5	103
194	COM18	-1868.75	286.5	19.5	103
195	COM20	-1901.25	286.5	19.5	103
196	COM22	-1933.75	286.5	19.5	103
197	COM24	-1966.25	286.5	19.5	103
198	COM26	-1998.75	286.5	19.5	103
199	COM28	-2031.25	286.5	19.5	103
200	COM30	-2063.75	286.5	19.5	103
201	COM32	-2096.25	286.5	19.5	103
202	COM34	-2128.75	286.5	19.5	103
203	COM36	-2161.25	286.5	19.5	103
204	COM38	-2193.75	286.5	19.5	103
205	COM40	-2226.25	286.5	19.5	103
206	COM42	-2258.75	286.5	19.5	103
207	COM44	-2291.25	286.5	19.5	103
208	COM46	-2323.75	286.5	19.5	103
209	COM48	-2356.25	286.5	19.5	103
210	COM50	-2388.75	286.5	19.5	103
211	COM52	-2421.25	286.5	19.5	103

TRAY INFORMATION



	Spec
W1	50.70±0.10(1996)
W2	45.70±0.10(1799)
H	3.95±0.10 (156)
E	2.20±0.05 (87)
Dx	4.45±0.05 (175)
TPx	41.80±0.10(1646)
Dy	6.33±0.05 (249)
TPy	38.04±0.10(1498)
Px	2.20±0.05 (87)
Py	6.34±0.05 (250)
X	0.94±0.05 (37)
Y	5.17±0.05 (204)
Z	0.55±0.05 (22)

<NOTE>
1. SURFACE RESISTANCE: 10 e 7~10 e11 ohm/SQ
2. MATERIAL: ABS WITH ESD PROTECTION, COLOR: BLACK
3. NO BURR AND FOREIGN MATERIAL(OIL) ON SURFACE OF CHIP TRAY.
4. MAKER OF CHIP TRAY SHOULD CLEAN THE SURFACE OF CHIP TRAY.
5. TRAY WARPAGE: Max. 0.1mm
6. We can put a piece of Lint free paper between the two trays.
7. The die thickness is 0.4 mm
8. The bottom of pocket:Rough pattern

Unless Otherwise Specified		ULTRACHIP INC. 晶宏半導體					
Unit	mm	2吋華丙萃 H20-37X204-22(140)				Scale	N/A
General Roughness	N/A					Package Code	N/A
Tolerance						Material	N/A
Dimension	see drawing detail		Drawn	Checked	Approved	Drawing No.	03-DWG-003-034
Angle	N/A	By:	Jack Chung	Jack Chung	Joan	Sheet	1 of 1
		Date	02-05-07	02-05-07	02-05-07	Size	A4
						Proj.	N/A
						Rev.	A

REVISION HISTORY

Revision	Contents	Date of Rev.
0.6	(First release)	Apr. 27, 2007