

*HIGH-VOLTAGE MIXED-SIGNAL IC*

**UC1608**

128COM x 240SEG Matrix LCD Controller-Driver

**MP Specifications**  
**Revision 1.1**

**November 4, 2004**

**ULTRACHIP**

*The Coolest LCD Driver. Ever!!*



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# UC1608

*Single-Chip, Ultra-Low Power  
128COM x 240SEG Matrix  
Passive LCD Controller-Driver*

## INTRODUCTION

UC1608 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power COM and SEG drivers, UC1608 contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

## MAIN APPLICATIONS

- Cellular Phones, Smart Phones, PDA and other battery operated palm top devices and/or portable Instruments

## FEATURE HIGHLIGHTS

- Single chip controller-driver supports 128 COM x 240 SEG LCD, with vertical scroll.
- Support both row ordered and column ordered display buffer RAM access.

- Support industry standard 3-wire, 4-wire serial bus (S9, S8, S8uc) and 8-bit/4-bit parallel bus (8080 or 6800).
- Support two multiplexing rates (128, 96).
- Self-configuring 8x charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Software programmable 4 temperature compensation coefficients.
- On-chip Power-ON Reset and Software RESET commands, make RST pin optional.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- $V_{DD}$  (digital) range: 2.7V ~ 3.3V  
 $V_{DD}$  (analog) range: 2.7V ~ 3.3V  
LCD  $V_{OP}$  range: 11.3V ~ 16V
- Available in gold bump dies  
Bump pitch: 45 $\mu$ M min.  
Bump gap: 18 $\mu$ M min.  
Bump surface: > 3000 $\mu$ M<sup>2</sup>

**ORDERING INFORMATION**

| Product ID | Description      |
|------------|------------------|
| UC1608xGBE | Gold bumped die. |
| UC1608xFBE | COF packaging.   |

**General Notes****APPLICATION INFORMATION**

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

**BARE DIE DISCLAIMER**

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post wafer saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into wafer pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

**LIFE SUPPORT APPLICATIONS**

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

**CONTENT DISCLAIMER**

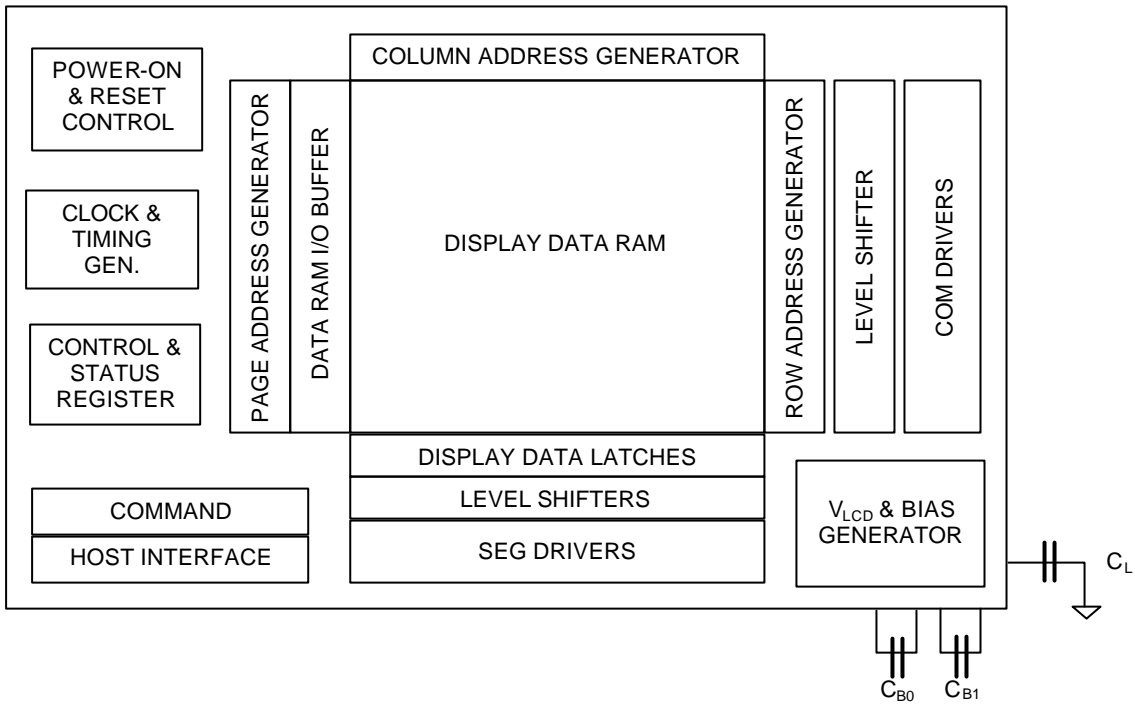
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**BLOCK DIAGRAM**



**PIN DESCRIPTION**

| Name   | Type | Pins             | Description   |
|--|------|------------------|---|
| <b>MAIN POWER SUPPLY</b>   |      |                  |   |
| V <sub>DD</sub><br>V <sub>DD2</sub><br>V <sub>DD3</sub>                      | PWR  | 5<br>5<br>3      | V <sub>DD</sub> is the digital V <sub>DD</sub> . V <sub>DD2</sub> /V <sub>DD3</sub> is the analog power supply and it should be connected to the same power source.<br>V <sub>DD</sub> supplies for digital logic and display data RAM. V <sub>DD2</sub> supplies for V <sub>LCD</sub> and V <sub>BIAS</sub> generator, V <sub>DD3</sub> supplies for other analog circuits.<br>Please maintain the following relationship:<br>$V_{DD} + 1.3V \geq V_{DD2/3} \geq V_{DD}$<br>Minimize the trace resistance for V <sub>DD</sub> and V <sub>DD2</sub> /V <sub>DD3</sub> . |
| V <sub>SS</sub><br>V <sub>SS2</sub>  | GND  | 4<br>5           | Ground. Connect V <sub>SS</sub> and V <sub>SS2</sub> to the shared GND pin.<br>Minimize the trace resistance for V <sub>SS</sub> and V <sub>SS2</sub> .   |
| <b>LCD POWER SUPPLY</b>  |      |                  |   |
| V <sub>BIAS</sub>  | I    | 1                | This is the reference voltage to generate the actual SEG driving voltage. V <sub>BIAS</sub> can be used to fine tune V <sub>LCD</sub> by external variable resistors. Internal resistor network has been provided to simplify external trimming circuit.<br>In COF application, connect a small bypass capacitor between V <sub>BIAS</sub> and V <sub>SS</sub> to reduce noise.   |
| V <sub>B1+</sub><br>V <sub>B1-</sub><br>V <sub>B0+</sub><br>V <sub>B0-</sub> | PWR  | 6<br>6<br>4<br>6 | LCD Bias Voltages. These are the voltage source to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C <sub>BX</sub> value between V <sub>BX+</sub> and V <sub>BX-</sub> .<br>The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimize the trace resistance is critical in achieving high quality image.  |
| V <sub>LCDIN</sub><br>V <sub>LCDOUT</sub>                                    | PWR  | 2<br>2           | Main LCD Power Supply. Connect these pins together.<br>A by-pass capacitor C <sub>L</sub> is optional. When C <sub>L</sub> is used, connect C <sub>L</sub> between V <sub>LCD</sub> and V <sub>SS</sub> , and keep the trace resistance under 300 .   |

**Note:**

Recommended capacitor values:

C<sub>B</sub>: 150~250x LCD load capacitance or 4.7μF (2V), whichever is higher.

C<sub>L</sub>: 50nF ~ 0.1μF (25V) is appropriate for most applications.

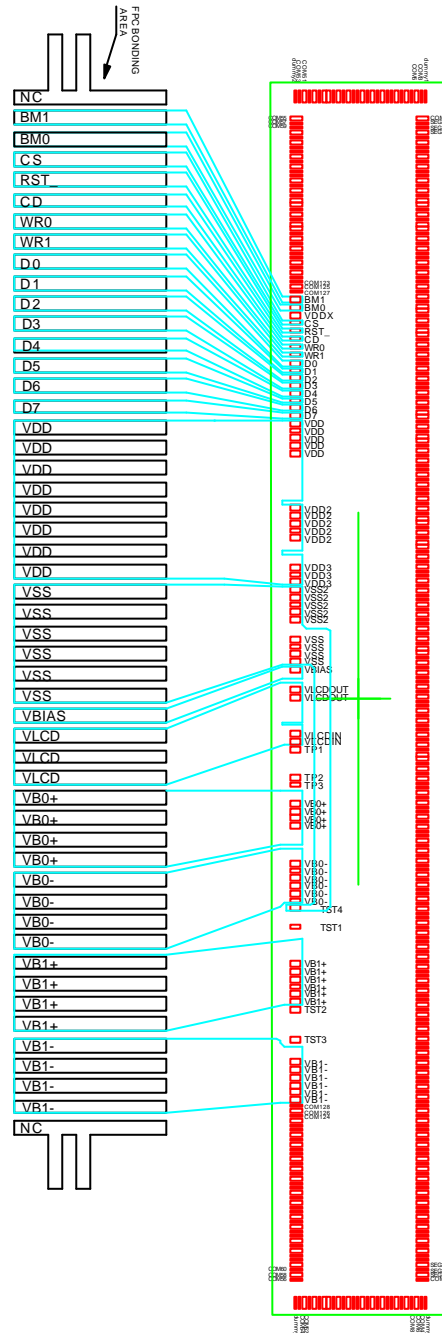


| Name                  | Type                | Pins   | Description   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
|-----------------------|---------------------|--|---|--------------------|---------------------|---------------------|---------------|--------------------|------------|----|-------|------------|-----|----|------------|-------|----|------------|----|----|---|----|----|---|----|-------|--|-----|----|----|---|---|---|----|----|---|---|---|----|----|---|----|---------|----|----|---|---|---|
| <b>HOST INTERFACE</b> |                     |  |   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| BM[1:0]               | I                   | 2  | <p>Bus mode: The interface bus mode is determined by BM[1:0] and D[7:6] by the following relationship:</p> <table border="1"> <thead> <tr> <th>BM[1:0]</th> <th>D[7:6]</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>11</td> <td>Data</td> <td>6800/8-bit</td> </tr> <tr> <td>10</td> <td>Data</td> <td>8080/8-bit</td> </tr> <tr> <td>01</td> <td>0X</td> <td>6800/4-bit</td> </tr> <tr> <td>00</td> <td>0X</td> <td>8080/4-bit</td> </tr> <tr> <td>01</td> <td>10</td> <td>3-wire SPI w/ 9-bit token<br/>(S9: conventional)</td> </tr> <tr> <td>00</td> <td>10</td> <td>4-wire SPI w/ 8-bit token<br/>(S8: conventional)</td> </tr> <tr> <td>00</td> <td>11</td> <td>3/4-wire SPI w/ 8-bit token<br/>(S8uc: Ultra-Compact)</td> </tr> </tbody> </table>  | BM[1:0]            | D[7:6]              | Mode                | 11            | Data               | 6800/8-bit | 10 | Data  | 8080/8-bit | 01  | 0X | 6800/4-bit | 00    | 0X | 8080/4-bit | 01 | 10 | 3-wire SPI w/ 9-bit token<br>(S9: conventional) | 00 | 10 | 4-wire SPI w/ 8-bit token<br>(S8: conventional) | 00 | 11    | 3/4-wire SPI w/ 8-bit token<br>(S8uc: Ultra-Compact) |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| BM[1:0]               | D[7:6]              | Mode   |   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| 11                    | Data                | 6800/8-bit   |   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| 10                    | Data                | 8080/8-bit   |   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| 01                    | 0X                  | 6800/4-bit   |   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| 00                    | 0X                  | 8080/4-bit   |   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| 01                    | 10                  | 3-wire SPI w/ 9-bit token<br>(S9: conventional)      |   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| 00                    | 10                  | 4-wire SPI w/ 8-bit token<br>(S8: conventional)      |   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| 00                    | 11                  | 3/4-wire SPI w/ 8-bit token<br>(S8uc: Ultra-Compact) |   |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| CS                    | I                   | 1  | Chip Select. The chip is selected when CS="H". When the chip is not selected, D[7:0] will be high impedance.  |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| RST                   | I                   | 1  | When RST="L", all control registers are re-initialized by their default states. Since UC1608 has built-in Power-ON-Reset and Software Reset command, RST pin is not required for proper chip operation. When RST is not used, connect the pin to V <sub>DD</sub> .  |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| CD                    | I                   | 1  | Select Control data or Display data for read/write operation. In S9 mode, CD pin is not used. Connect CD to V <sub>SS</sub> when not used.<br>"L": Control data      "H": Display data  |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| WR0<br>WR1            | I                   | 2  | WR[1:0] controls the read/write operation of the host interface. See Host Interface section for more detail.<br>In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V <sub>SS</sub> .  |                    |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| D0~D7                 | I/O                 | 8  | <p>Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,</p> <table border="1"> <thead> <tr> <th></th> <th>BM=1x<br/>(Parallel)</th> <th>BM=0x<br/>(Parallel)</th> <th>BM=01<br/>(S9)</th> <th>BM=00<br/>(S8/S8uc)</th> </tr> </thead> <tbody> <tr> <td>D0</td> <td>D0</td> <td>D0/D4</td> <td>SCK</td> <td>SCK</td> </tr> <tr> <td>D1</td> <td>D1</td> <td>D1/D5</td> <td>-</td> <td>-</td> </tr> <tr> <td>D2</td> <td>D2</td> <td>D2/D6</td> <td>-</td> <td>-</td> </tr> <tr> <td>D3</td> <td>D3</td> <td>D3/D7</td> <td>SDA</td> <td>SDA</td> </tr> <tr> <td>D4</td> <td>D4</td> <td>-</td> <td>-</td> <td>-</td> </tr> <tr> <td>D5</td> <td>D5</td> <td>-</td> <td>-</td> <td>-</td> </tr> <tr> <td>D6</td> <td>D6</td> <td>-</td> <td>S9</td> <td>S8/S8uc</td> </tr> <tr> <td>D7</td> <td>D7</td> <td>0</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Connect unused pins to V<sub>DD</sub> or V<sub>SS</sub>.</p> |                    | BM=1x<br>(Parallel) | BM=0x<br>(Parallel) | BM=01<br>(S9) | BM=00<br>(S8/S8uc) | D0         | D0 | D0/D4 | SCK        | SCK | D1 | D1         | D1/D5 | -  | -          | D2 | D2 | D2/D6   | -  | -  | D3  | D3 | D3/D7 | SDA  | SDA | D4 | D4 | - | - | - | D5 | D5 | - | - | - | D6 | D6 | - | S9 | S8/S8uc | D7 | D7 | 0 | 1 | 1 |
|                       | BM=1x<br>(Parallel) | BM=0x<br>(Parallel)                                  | BM=01<br>(S9)   | BM=00<br>(S8/S8uc) |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| D0                    | D0                  | D0/D4  | SCK   | SCK                |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| D1                    | D1                  | D1/D5  | -   | -                  |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| D2                    | D2                  | D2/D6  | -   | -                  |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| D3                    | D3                  | D3/D7  | SDA   | SDA                |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| D4                    | D4                  | -  | -   | -                  |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| D5                    | D5                  | -  | -   | -                  |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| D6                    | D6                  | -  | S9  | S8/S8uc            |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |
| D7                    | D7                  | 0  | 1   | 1                  |                     |                     |               |                    |            |    |       |            |     |    |            |       |    |            |    |    |   |    |    |   |    |       |  |     |    |    |   |   |   |    |    |   |   |   |    |    |   |    |         |    |    |   |   |   |

| Name                     | Type | Pins | Description   |
|--------------------------|------|------|---|
| <b>LCD DRIVER OUTPUT</b> |      |      |   |
| SEG1 ~<br>SEG240         | HV   | 240  | SEG (column) driver outputs. Support up to 240 columns. Leave unused drivers open-circuit.  |
| COM1 ~<br>COM128         | HV   | 128  | COM (row) driver outputs. Support up to 128 rows. When Mux Rate is not 128, please use only COM1–COM(x), x=128, or 96, and leave COM (x+1) ~ COM128 open-circuit.   |
| <b>Misc. PINS</b>        |      |      |   |
| V <sub>DDX</sub>         |      | 1    | Auxiliary V <sub>DD</sub> . These pins are connected to the main V <sub>DD</sub> bus on chip, and they are provided to facilitate chip packaging in COG and COF applications. There is no need to connect V <sub>DDX</sub> to V <sub>DD</sub> externally. These pins should not be used to provide V <sub>DD</sub> power to the chip. |
| TST4                     | I    | 1    | Test control. Connect to V <sub>SS</sub> for normal operation.  |
| TST[3:1]                 | I/O  | 3    | Test I/O pins. Leave these pins open circuit during normal use.   |
| TP[3:1]                  | I    | 3    | Leave these pins open circuit during normal use.  |

**Note:** Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM<sub>X</sub> or SEG<sub>X</sub> will correspond to index X-1, and the value ranges for those index registers will be 0~127 for COM and 0~239 for SEG.

REFERENCE COG LAYOUT



Notes for V<sub>DD</sub> with COG:

- The typical operation condition of UC1608, V<sub>DD</sub>=2.7V, should be met under all operating conditions. Unless V<sub>DD</sub> and V<sub>DD2/3</sub> ITO trances can each be controlled to be 5 Ω or lower; otherwise V<sub>DD</sub>-V<sub>DD2/3</sub> separation can cause the actual on-chip V<sub>DD</sub> to drop below V<sub>DD</sub>=2.6V during high speed data write condition. Therefore, for COG, V<sub>DD</sub>-V<sub>DD2/3</sub> separation requires very careful ITO layout and very stringent testing before MP.
- Keep V<sub>DD</sub> and V<sub>SS</sub> under 150Ω.

**CONTROL REGISTERS**

UC1608 contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meaning and their default value. The commands supported by UC1608 are described in the next two sections, first a summary table, followed by a detailed description.

*Name:* The Symbolic reference of the register byte.  
 Note that, some symbol names refer to collection of bits (flags) within one register byte.

*Default:* Numbers shown in **Bold** fonts are values after *Power-Up-Reset* and *System-Reset*.

| Name | Bits | Default | Description  |
|------|------|---------|--|
| SL   | 6    | 0H      | Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (127– 2xFL). Setting SL outside of this range causes undefined effect on the displayed image.  |
| FL   | 4    | 0H      | Fixed Lines. The first FLx2 lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable.   |
| CR   | 8    | 0H      | Return Column Address. Useful for cursor implementation.   |
| CA   | 8    | 0H      | Display Data RAM Column Address<br>(Used in Host to Display Data RAM access)   |
| PA   | 4    | 0H      | Display Data RAM Page Address<br>(Used in Host to Display Data RAM access)   |
| BR   | 2    | 2H      | Bias Ratio. The ratio between $V_{LCD}$ and $V_{BIAS}$<br>00b= 10.7      01b= 11.3<br><b>10b= 12.0</b> 11b= 12.7   |
| TC   | 2    | 0H      | Temperature Compensation (per °C).<br><b>00b: 0.0%</b> 01b: -0.05%<br>10b: -0.1%      11b: -0.2%   |
| GN   | 2    | 3H      | Gain, coarse setting of $V_{BIAS}$ and $V_{LCD}$   |
| PM   | 6    | 0H      | Electronic Potentiometer to fine tune $V_{BIAS}$ and $V_{LCD}$   |
| MR   | 1    | 1H      | Multiplexing Rate: Number of pixel rows:<br>0b: 96 <b>1b: 128</b>  |
| OM   | 2    | –       | Operating Modes (Read Only)<br>00b: Reset      01b: (Not used)<br>10b: Sleep      11b: Normal  |
| BZ   | 1    | –       | Busy with internal processes (reset, changing mode, etc.)<br>OK for Display RAM read/write access.   |
| RS   | 1    | –       | Reset in progress, Host Interface not ready  |
| PC   | 3    | 5H      | Power Control.<br>PC[1:0]: Panel Loading<br>00b: LCD < 26nF <b>01b: 26nF &lt; LCD &lt; 43nF</b><br>10b: 43nF < LCD < 60nF      11b: 60nF < LCD < 90nF<br>For COG module, the ITO substrate for SEG plate and COM routing:<br>15 /Sq    15nF < LCD < 35nF.<br>10 /Sq    35nF < LCD < 50nF<br>7 /Sq    50nF < LCD < 75nF<br>PC[2]: Pump Control<br>0b: External $V_{LCD}$ <b>1b: Internal <math>V_{LCD}</math></b> |
| DC   | 3    | 0H      | Display Control:<br>DC[0]: PXV: Pixels Inverse (Default <b>0: OFF</b> )  |

| Name | Bits | Default | Description   |
|------|------|---------|---|
|      |      |         | DC[1]: APO: All Pixels ON (Default <b>0</b> : <b>OFF</b> )<br>DC[2]: Display ON/OFF (Default <b>0</b> : <b>OFF</b> ).   |
| AC   | 4    | 1H      | Address Control:<br>AC[0]: WA: Automatic column/page Wrap Around (Default <b>1</b> : <b>ON</b> )<br>AC[1]: Reserved (always set to <b>0</b> )<br>AC[2]: PID: PA (page address) auto increment direction ( <b>0</b> : +1 1: -1)<br>AC[3]: CUM: Cursor update mode, (Default <b>0</b> : <b>OFF</b> )<br>when CUM=1, CA increment on write only, wrap around suspended |
| LC   | 4    | 0H      | LCD Mapping Control:<br>LC[0]: MSF: MSB First mapping Option (Default <b>0</b> : <b>OFF</b> )<br>LC[1]: Reserved (always set to <b>0</b> )<br>LC[2]: MX, Mirror X (Column sequence inversion) (Default <b>0</b> : <b>OFF</b> )<br>LC[3]: MY, Mirror Y (Row sequence inversion) (Default <b>0</b> : <b>OFF</b> )   |
| APC0 | 8    | 2AH     | Advanced Product Configuration. For UltraChip only. Please do not use.  |
| APC1 | 4    | EH      | Advanced Product Configuration. For UltraChip only. Please do not use.  |

**COMMAND TABLE**

The following is a list of host commands supported by UC1608

C/D: 0: Control, 1: Data  
 W/R: 0: Write Cycle, 1: Read Cycle  
 # Useful Data bits  
 – Don't Care

|    | Command   | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2  | D1  | D0 | Action                             | Default           |
|----|---|-----|-----|----|----|----|----|----|-----|-----|----|------------------------------------|-------------------|
| 1  | Write Data Byte                                     | 1   | 0   | #  | #  | #  | #  | #  | #   | #   | #  | Write 1 byte                       | N/A               |
| 2  | Read Data Byte                                      | 1   | 1   | #  | #  | #  | #  | #  | #   | #   | #  | Read 1 byte                        | N/A               |
| 3  | Get Status  | 0   | 1   | BZ | MX | DE | RS | WA | GN1 | GN0 | 1  | Get Status                         | N/A               |
| 4  | Set Column Address LSB                              | 0   | 0   | 0  | 0  | 0  | 0  | #  | #   | #   | #  | Set CA[3:0]                        | 0                 |
|    | Set Column Address MSB                              | 0   | 0   | 0  | 0  | 0  | 1  | #  | #   | #   | #  | Set CA[7:4]                        | 0                 |
| 5  | Set Mux Rate and temperature compensation.          | 0   | 0   | 0  | 0  | 1  | 0  | 0  | #   | #   | #  | Set {MR, TC[1:0]}                  | MR: 1b<br>TC: 00b |
| 6  | Set Power Control                                   | 0   | 0   | 0  | 0  | 1  | 0  | 1  | #   | #   | #  | Set PC[2:0]                        | 101b              |
| 7  | Set Adv. Program Control.<br>(double byte command)  | 0   | 0   | 0  | 0  | 1  | 1  | 0  | 0   | 0   | R  | For UltraChip only.<br>Do not use. | N/A               |
|    |   | 0   | 0   | #  | #  | #  | #  | #  | #   | #   | #  |                                    |                   |
| 8  | Set Start Line                                      | 0   | 0   | 0  | 1  | #  | #  | #  | #   | #   | #  | Set SL[5:0]                        | 0                 |
| 9  | Set Gain and Potentiometer<br>(double-byte command) | 0   | 0   | 1  | 0  | 0  | 0  | 0  | 0   | 0   | 1  | Set {GN[1:0],<br>PM[5:0]}          | GN=3<br>PM=0      |
|    |   | 0   | 0   | #  | #  | #  | #  | #  | #   | #   | #  |                                    |                   |
| 10 | Set RAM Address Control                             | 0   | 0   | 1  | 0  | 0  | 0  | 1  | #   | #   | #  | Set AC[2:0]                        | 001b              |
| 11 | Set All-Pixel-ON                                    | 0   | 0   | 1  | 0  | 1  | 0  | 0  | 1   | 0   | #  | Set DC[1]                          | 0=disable         |
| 12 | Set Inverse Display                                 | 0   | 0   | 1  | 0  | 1  | 0  | 0  | 1   | 1   | #  | Set DC[0]                          | 0=disable         |
| 13 | Set Display Enable                                  | 0   | 0   | 1  | 0  | 1  | 0  | 1  | 1   | 1   | #  | Set DC[2]                          | 0=disable         |
| 14 | Set Fixed Lines                                     | 0   | 0   | 1  | 0  | 0  | 1  | #  | #   | #   | #  | Set FL[3:0]                        | 0                 |
| 15 | Set Page Address                                    | 0   | 0   | 1  | 0  | 1  | 1  | #  | #   | #   | #  | Set PA[3:0]                        | 0                 |
| 16 | Set LCD Mapping Control                             | 0   | 0   | 1  | 1  | 0  | 0  | #  | #   | #   | #  | Set LC[3:0]                        | 0                 |
| 17 | System Reset  | 0   | 0   | 1  | 1  | 1  | 0  | 0  | 0   | 1   | 0  | System Reset                       | N/A               |
| 18 | NOP   | 0   | 0   | 1  | 1  | 1  | 0  | 0  | 0   | 1   | 1  | No operation                       | N/A               |
| 19 | Set LCD Bias Ratio                                  | 0   | 0   | 1  | 1  | 1  | 0  | 1  | 0   | #   | #  | Set BR[1:0]                        | 10b=12            |
| 20 | Reset Cursor Mode                                   | 0   | 0   | 1  | 1  | 1  | 0  | 1  | 1   | 1   | 0  | AC[3]=0, CA=CR                     | N/A               |
| 21 | Set Cursor Mode                                     | 0   | 0   | 1  | 1  | 1  | 0  | 1  | 1   | 1   | 1  | AC[3]=1, CR=CA                     | N/A               |
| 22 | Set Test Control<br>(double byte command)           | 0   | 0   | 1  | 1  | 1  | 0  | 0  | 1   | TT  |    | For UltraChip only.<br>Do not use. | N/A               |
|    |   | 0   | 0   | #  | #  | #  | #  | #  | #   | #   | #  |                                    |                   |

\* Other than commands listed above, all other bit patterns may result in undefined behavior.

## COMMAND DESCRIPTION

### (1) Write data to display memory

| Action     | C/D | W/R | D7                       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|--------------------------|----|----|----|----|----|----|----|
| Write data | 1   | 0   | 8bits data write to SRAM |    |    |    |    |    |    |    |

### (2) Read data to display memory

| Action    | C/D | W/R | D7                   | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------|-----|-----|----------------------|----|----|----|----|----|----|----|
| Read data | 1   | 1   | 8bits data from SRAM |    |    |    |    |    |    |    |

Write/Read Data Byte (command 1,2) operations access display buffer RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will be incremented automatically depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of page (MC), and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches end of page, CA will be reset to 0 and PA will be increased or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 15), PA will be wrapped around to the other end of RAM and continue.

### (3) Get Status

| Action     | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2  | D1  | D0 |
|------------|-----|-----|----|----|----|----|----|-----|-----|----|
| Get Status | 0   | 1   | BZ | MX | DE | RS | WA | GN1 | GN0 | 1  |

Status flag definitions:

*BZ*: Busy with internal process.

*MX*: Status of register LC[2], mirror X.

*DE*: Display enable flag. DE=1 when display enabled

*RS*: Reset in progress. If RS=1, host interface will be inaccessible.

*WA*: status of register AC[0]. Automatic column/page wrap around.

*GN0, 1*: GN[1:0]. register Gain

### (4) Set Column Address

| Action                         | C/D | W/R | D7 | D6 | D5 | D4 | D3  | D2  | D1  | D0  |
|--------------------------------|-----|-----|----|----|----|----|-----|-----|-----|-----|
| Set Column Address LSB CA[3:0] | 0   | 0   | 0  | 0  | 0  | 0  | CA3 | CA2 | CA1 | CA0 |
| Set Column Address MSB CA[7:4] | 0   | 0   | 0  | 0  | 0  | 1  | CA7 | CA6 | CA5 | CA4 |

Set the SRAM column address before Write/Read memory from host interface.

CA possible value=**0-239**

### (5) Set Multiplex Rate and Temperature Compensation

| Action                               | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1  | D0  |
|--------------------------------------|-----|-----|----|----|----|----|----|----|-----|-----|
| Set Multiplex Rate MR                | 0   | 0   | 0  | 0  | 1  | 0  | 0  | MR | TC1 | TC0 |
| Set Temperature Compensation TC[1:0] | 0   | 0   | 0  | 0  | 1  | 0  | 0  | MR | TC1 | TC0 |

Set the multiplex ratio (number of rows) and temperature compensation.

MUX ratio definition:   0b=96                   **1b=128**

Temperature compensation curve definition:

**00b= -0.00%/C**   01b= -0.05%/C   10b= -0.10%/C   11b= -0.20%/C

**(6) Set Power Control**

| Action                    | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2  | D1  | D0  |
|---------------------------|-----|-----|----|----|----|----|----|-----|-----|-----|
| Set Panel Loading PC[2:0] | 0   | 0   | 0  | 0  | 1  | 0  | 1  | PC2 | PC1 | PC0 |

Set PC[1:0], according to the capacitance loading of LCD panel.

Panel loading definition:

00b: LCD < 26 nF

**01b: 26 nF < LCD < 43 nF**

10b: 43 nF < LCD < 60nF

**11b: 60nF < LCD < 90 nF**

Set PC[2] to program to use internal charge pump of external V<sub>LCD</sub> source.

Pump control definition:

0b=External V<sub>LCD</sub>

**1b=Internal V<sub>LCD</sub>**

**(7) Set Advanced Program Control**

| Action                | C/D | W/R | D7                     | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|------------------------|----|----|----|----|----|----|----|
| Set APC[0]            | 0   | 0   | 0                      | 0  | 1  | 1  | 0  | 0  | 0  | R  |
| (Double byte command) | 0   | 0   | APC register parameter |    |    |    |    |    |    |    |

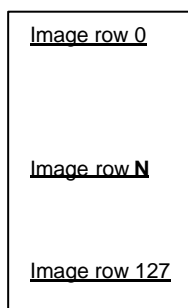
For UltraChip only. Please Do NOT use.

**(8) Set Start Line**

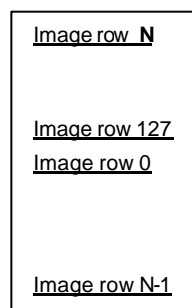
| Action                 | C/D | W/R | D7 | D6 | D5  | D4  | D3  | D2  | D1  | D0  |
|------------------------|-----|-----|----|----|-----|-----|-----|-----|-----|-----|
| Set Start Line SL[5:0] | 0   | 0   | 0  | 1  | SL5 | SL4 | SL3 | SL2 | SL1 | SL0 |

Set the start line number

Start line setting will scroll the displayed image up by SL rows. The valid value is between 0 (no scrolling) and 63. One example of the visual effect on LCD is illustrated in the figure below.



SL=0



SL=N

**(9) Set Gain and Potentiometer**

| Action  | C/D | W/R | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|---|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Set Gain and Potentiometer<br>GN [1:0] PM [5:0] | 0   | 0   | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| (Double byte command)                           | 0   | 0   | GN1 | GN0 | PM5 | PM4 | PM3 | PM2 | PM1 | PM0 |

Program Gain (GN[1:0]) and Potentiometer (PM[5:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range of GN = 0 ~ 3

PM value = 0 ~ 63



**(10) Set RAM Address Control**

| Action       | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2  | D1  | D0  |
|--------------|-----|-----|----|----|----|----|----|-----|-----|-----|
| Set AC [2:0] | 0   | 0   | 1  | 0  | 0  | 0  | 1  | AC2 | AC1 | AC0 |

Program registers AC[2:0] for RAM address control.

AC[0] - WA, Automatic column/page wrap around.

0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary

1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increment by one step.

AC[1] – Reserved (always set to 0)

AC[2] – PID, page address (PA) auto increment direction ( 0/1 = +/- 1 )

When WA=1, controls whether page address will be adjusted by +1 or -1, when CA reached CA boundary.

No effect when WA=0.

CA boundary is 239 and PA boundary is 15 when PID=0, PA boundary is 0 when PID=1.

**(11) Set All Pixel ON**

| Action                  | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0  |
|-------------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Set All Pixel On DC [1] | 0   | 0   | 1  | 0  | 1  | 0  | 0  | 1  | 0  | DC1 |

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

**(12) Set Inverse Display**

| Action                     | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0  |
|----------------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Set Inverse Display DC [0] | 0   | 0   | 1  | 0  | 1  | 0  | 0  | 1  | 1  | DC0 |

Set DC[0] to force all SEG drivers to output the inverse of the data stored in display memory. This function has no effect on the existing data stored in display RAM.

**(13) Set Display Enable**

| Action                   | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0  |
|--------------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Set Display Enable DC[2] | 0   | 0   | 1  | 0  | 1  | 0  | 1  | 1  | 1  | DC2 |

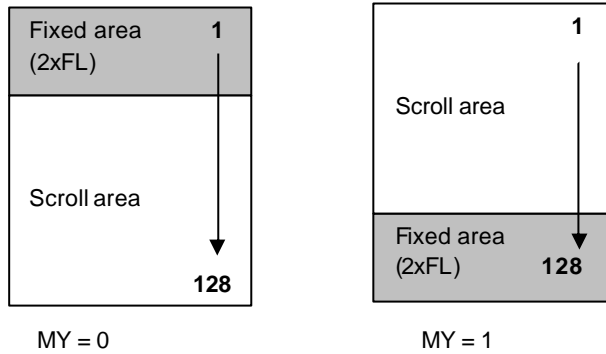
This command is for programming registers DC[2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1608 will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

**(14) Set Fixed Lines**

| Action                   | C/D | W/R | D7 | D6 | D5 | D4 | D3  | D2  | D1  | D0  |
|--------------------------|-----|-----|----|----|----|----|-----|-----|-----|-----|
| Set Fixed Lines FL [3:0] | 0   | 0   | 1  | 0  | 0  | 1  | FL3 | FL2 | FL1 | FL0 |

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFL rows for mirror Y (MY) is 0 and bottom 2xFL rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



**(15) Set Page Address**

| Action                        | C/D | W/R | D7 | D6 | D5 | D4 | D3  | D2  | D1  | D0  |
|-------------------------------|-----|-----|----|----|----|----|-----|-----|-----|-----|
| Set Page Address LSB PA [3:0] | 0   | 0   | 1  | 0  | 1  | 1  | PA3 | PA2 | PA1 | PA0 |

Set the SRAM page address before write/read memory from host interface.  
Effective range of value = 0 ~ 15

**(16) Set LCD Mapping Control**

| Action                          | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0  |
|---------------------------------|-----|-----|----|----|----|----|----|----|----|-----|
| Set LCD Mapping Control LC[3:0] | 0   | 0   | 1  | 1  | 0  | 0  | MY | MX | 0  | MSF |

Set LC[3:0] for COM (row) mirror (MY), SEG (column) mirror (MX) and MSB first or LSB first options (MSF).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 239-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

MSF is implemented by MSB-LSB swapping. When MSB first (LC[0]) bit is set, data D[7:0] will be re-aligned as D[0:7] then be stored to RAM.

**(17) System Reset**

| Action       | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------|-----|-----|----|----|----|----|----|----|----|----|
| System Reset | 0   | 0   | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 0  |

This command will activate the system reset. The system will take about 15ms to reset

**(18) NOP**

| Action       | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------|-----|-----|----|----|----|----|----|----|----|----|
| No operation | 0   | 0   | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 1  |

This command is used for "no operation".

**(19) Set LCD Bias Ratio**

| Action                  | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1  | D0  |
|-------------------------|-----|-----|----|----|----|----|----|----|-----|-----|
| Set Bias Ratio BR [1:0] | 0   | 0   | 1  | 1  | 1  | 0  | 1  | 0  | BR1 | BR0 |

Bias ratio definition:

00b= 10.7      01b=11.3      **10b=12.0**      11b=12.7

**(20) Reset Cursor Mode**

| Action                           | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|-----|-----|----|----|----|----|----|----|----|----|
| Return to Cursor. AC[3]=0, CA=CR | 0   | 0   | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  |

This command is used to reset cursor update mode function. See description below.

**(21) Set Cursor Mode**

| Action            | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------|-----|-----|----|----|----|----|----|----|----|----|
| Set AC[3]=1 CR=CA | 0   | 0   | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  |

Set Cursor Mode command is used to turn on cursor update mode function. AC[3] will be set to 1, register CR will be set to the value of register CA

When AC[3]=1, column address (CA) will only increment with write RAM operation but not on read RAM operation. The address CA wraps around will also be suspended no matter what WA setting is. The purpose of this combination of features is to support "Read-Modify-Write" for cursor implementation.

Reset Cursor Mode command will clear cursor update mode flag (AC[3]=0), CA will be restored to previous CA value which is stored in CR, and CA, PA increment will return to its normal condition.

**(22) Set Test Control**

| Action                | C/D | W/R | D7                | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-----|-----|-------------------|----|----|----|----|----|----|----|
| Set TT                | 0   | 0   | 1                 | 1  | 1  | 0  | 0  | 1  | TT |    |
| (Double byte command) | 0   | 0   | Testing parameter |    |    |    |    |    |    |    |

This command is used for UltraChip production testing. For UltraChip Only. Please do not use.

**LCD VOLTAGE SETTING**

**MULTIPLEX RATES**

Multiplex Rates (*MR*) is software programmable. Two MR is supported: 96, 128.

**BIAS RATIO SELECTION**

Bias Ratio (*BR*) is defined as the ratio between  $V_{LCD}$  and  $V_{BIAS}$ , i.e.

$$BR = V_{LCD} / V_{BIAS},$$

where  $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$ .

The theoretical optimum *Bias Ratio* can be estimated by  $\sqrt{MUX} + 1$ . In some applications, *BR* is set to be 10~15% lower than the optimum value calculated above in order to lower  $V_{LCD}$  by 5~6%. Such setting generally will not cause visible change in image quality.

UC1608 supports four *BR* as listed below. *BR* can be selected by software program.

| BR         | 0    | 1    | 2  | 3    |
|------------|------|------|----|------|
| Bias Ratio | 10.7 | 11.3 | 12 | 12.7 |

**Table 1:** Bias Ratios

**TEMPERATURE COMPENSATION**

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

| TC       | 0   | 1     | 2     | 3     |
|----------|-----|-------|-------|-------|
| % per °C | 0.0 | -0.05 | -0.10 | -0.20 |

**Table 2:** Temperature Compensation

**$V_{LCD}$  GENERATION**

$V_{LCD}$  may be supplied either by internal charge pump or by external power supply. The source of  $V_{LCD}$  is controlled by PC[2]. For good product performance it is recommended to keep  $V_{LCD}$  under 15.5V at room temperature.

When  $V_{LCD}$  is generated internally, the voltage level of  $V_{LCD}$  is determined by four control registers: *BR* (Bias Ratio), *GN* (Gain), *PM* (Potentiometer), and *TC* (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T \%)$$

where

$C_{V0}$  and  $C_{PM}$  are two constants, whose value depends on the *BR-GN* register setting. The values are provided in the table on next page,

*PM* is the numerical value of *PM* register,

*T* is the ambient temperature in °C, and

$C_T$  is the temperature compensation coefficient as selected by *TC* register.

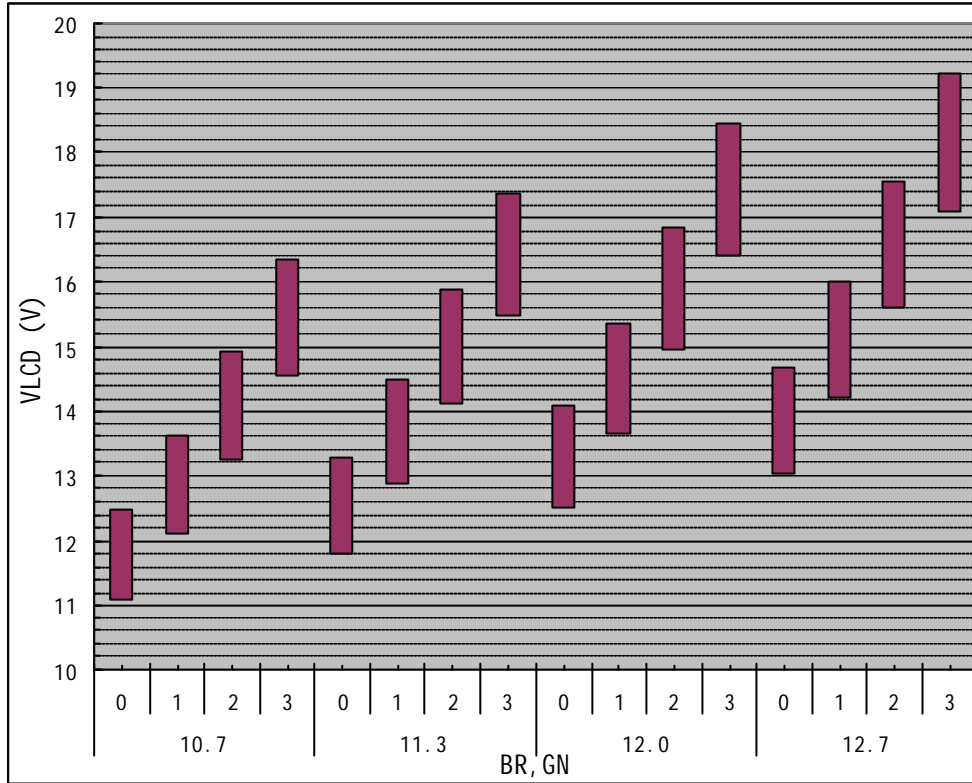
**ITO LAYOUT FOR COG MODULES**

When designing COG LCM, use lower resistance ITO glass for the SEG substrate to minimize SEG waveform crosstalk and minimize  $V_{DD}$ ,  $V_{SS}$  ITO trace resistance. In addition, COM trace resistance and the SEG-COM crossover resistance should also be minimize.

The power supply circuit of UC1608 is designed to handle LCD panels with loading up to ~50nF using 10- /Sq ITO glass with  $V_{D2/3} \geq 2.7V$ . For larger LCD panels use lower resistance ITO glass or COF packaging.

Due to crosstalk consideration, ~50nF is also the recommended maximum LCD panel size for COG applications, unless 7- /Sq or lower resistance ITO glass is used for the SEG substrate.

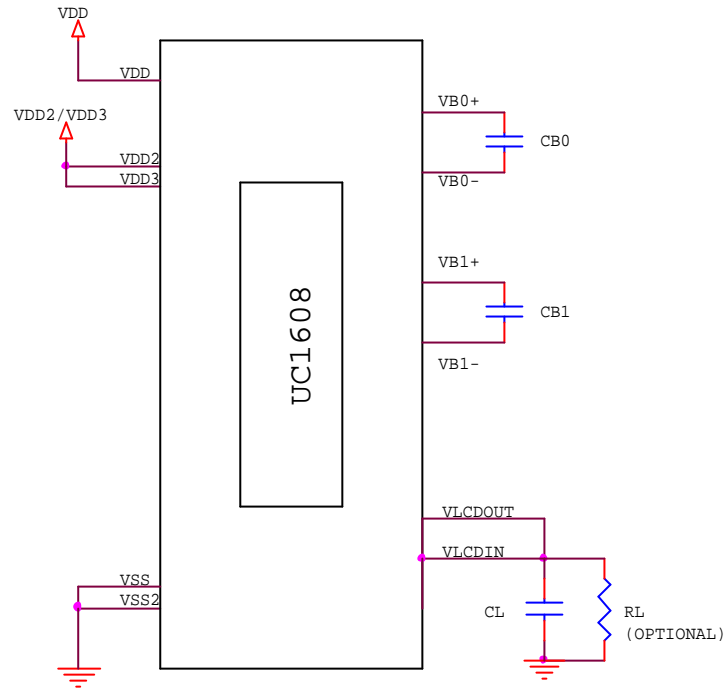
**V<sub>LCD</sub> QUICK REFERENCE**



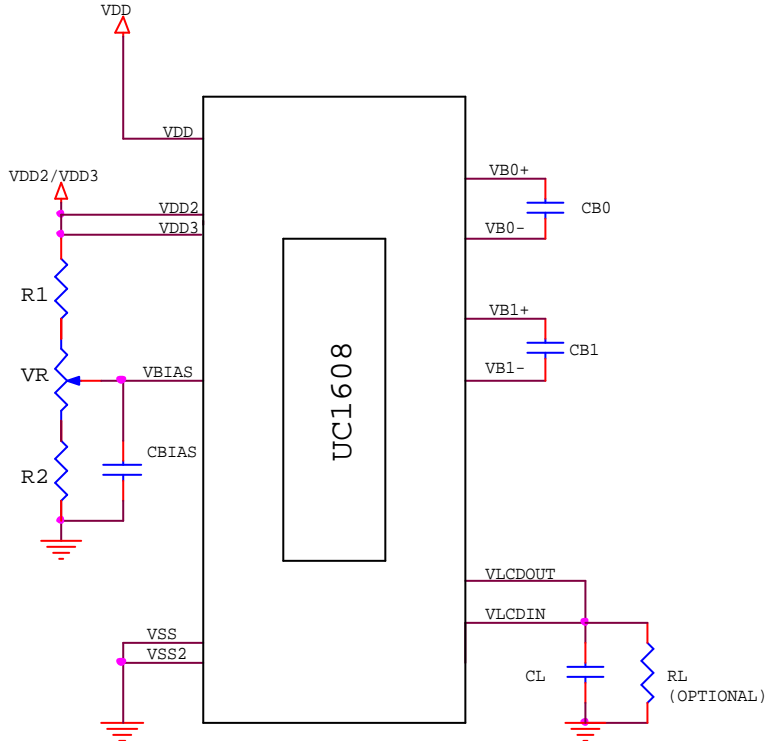
| BR   | GN | C <sub>V0</sub> (V) | C <sub>PM</sub> (mV) | VLCD Range (V) |        |
|------|----|---------------------|----------------------|----------------|--------|
|      |    |                     |                      | PM=00H         | PM=3FH |
| 10.7 | 0  | 11.09               | 22.12                | 11.09          | 12.48  |
|      | 1  | 12.10               | 24.19                | 12.10          | 13.63  |
|      | 2  | 13.27               | 26.51                | 13.27          | 14.94  |
|      | 3  | 14.55               | 28.44                | 14.55          | 16.34  |
| 11.3 | 0  | 11.79               | 23.56                | 11.79          | 13.28  |
|      | 1  | 12.87               | 25.66                | 12.87          | 14.49  |
|      | 2  | 14.12               | 28.01                | 14.12          | 15.88  |
|      | 3  | 15.46               | 30.37                | 15.46          | 17.38  |
| 12   | 0  | 12.51               | 24.91                | 12.51          | 14.08  |
|      | 1  | 13.65               | 27.05                | 13.65          | 15.36  |
|      | 2  | 14.96               | 29.77                | 14.96          | 16.84  |
|      | 3  | 16.40               | 32.34                | 16.40          | 18.44  |
| 12.7 | 0  | 13.03               | 25.89                | 13.03          | 14.66  |
|      | 1  | 14.22               | 28.17                | 14.22          | 15.99  |
|      | 2  | 15.59               | 31.14                | 15.59          | 17.55  |
|      | 3  | 17.09               | 33.64                | 17.09          | 19.21  |

**Note:** For best product reliability, keep V<sub>LCD</sub> under 16V under all temperature.

**Hi-V GENERATOR CIRCUIT**



**FIGURE 1:** Reference circuit using internal Hi-V generator circuit



**Figure 2:** Reference circuit using external Bias source

**Note :**

- Recommended component values:
  - $C_B$ : 150 ~250x LCD load capacitance or 4.7 $\mu$ F (2V), whichever is higher.
  - $C_L$ : 50nF ~ 0.1  $\mu$ F (25V) is appropriate for most applications.
  - $R_L$ : 10MO. Acts as a draining circuit when the power is abnormally shut down.
  - $V_R$ : 1MO.
  - $R_1, R_2$ : See instructions below.
  - $C_{BIAS}$ : 10nF ~ 0.1  $\mu$ F is recommended.
- The above component values are for reference only. Please optimize the values for the individual requirements of each specific application.
- To ensure consistency of LCM contrast, VLCD fine tuning is highly recommended.

Since the value of  $R_1/R_2$  depends strongly on the GN, PM, BR settings, and vary slightly depends on the value of  $V_{DD2}$ , each LCM design will need to be optimized individually.

The following is the recommended procedures for selecting  $R_1$ ,  $R_2$  and  $V_R$  values.

- Step 1: Adjust LCM for the best contrast with  $C_{BIAS}$ , but without  $R_1$ ,  $R_2$ ,  $V_R$ .
- Step 2: Measure  $V_{BIAS}$  voltage
- Step 3: Select  $V_R$  and  $R_2$  (recommend to start with  $V_R=1MO$ ,  $R_2=200K$ )
- Step 4: Calculate  $R_1$  by:  $R_1 = R_2 \times (V_{DD2}/V_{BIAS} - 1)$
- Step 5: Install  $R_1$ ,  $R_2$ ,  $V_R$ . The "neutral position" of  $V_R$  is at  $V_{BIAS}/V_{DD2}$ .
- Step 6: Test the fine tuning range by adjusting  $V_R$  over the full range.
- Step 7: If adjustment range is too narrow, reduce  $R_2$ , ... and vice versa.
- Step 8: Repeat from Step 4.

- Step 2, Measure  $V_{BIAS}$ , is a very critical step. Since the purpose of this circuit is to maximize the contrast consistency of mass production units, please fine tuning GN, PM, BR across at least 150~200 LCM units (without the  $V_{LCD}$  adjustment circuit), before finalizing the values of PM, GN, BR. The average  $V_{BIAS}$  should be measured after PM, GN and BR is selected and finalized.
- Please note that, the "Neutral position" of the  $V_R$  (the position with minimum  $V_{LCD}$  adjustment) is not the center, but located at  $V_{BIAS}/V_{DD2}$ . Relative to this "Neutral position", the circuit produced by above procedure will have equal  $V_{LCD}$  adjustment range of +N% ~ -N% for the average  $V_{LCD}$ .
- Please avoid situations where the adjustment of the  $V_R$  can push UC1608 out of its safe  $V_{LCD}$  operation range (16V) at the low end of operating temperature range. If this happens, then it will be possible for the MP operators to damage the LCM by adjusting the  $V_R$ .
- Since the value of  $V_{DD2}$  can affect the adjustment of the  $V_R$ , please apply  $V_{DD2}$  that is intended to be used in the final application during the mass production  $V_{LCD}$  tuning process.
- Due to its minor sensitivity to the value of  $V_{DD2}$ , this  $V_{LCD}$  tuning circuit may not be suitable for "standard product" where the actual  $V_{DD2}$  value can vary far over 5% from the design  $V_{DD2}$  value. For such applications, please use a Zener diode, such as Hitachi HZU3LL, to replace  $V_{DD2}$  as the power source for this  $V_{LCD}$  fine tuning circuit.

## LCD DISPLAY CONTROLS

### CLOCK & TIMING GENERATOR

UC1608 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

### DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When COM drivers are in idle mode, their outputs are high-impedance (open circuit). When SEG drivers are in idle mode, their outputs are connected to  $V_{SS}$ .

### DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where  $x=1\sim 128$ , refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is the same for all MR, MX and MY settings. When MR is not 128, then COM(x) ~ COM128 ( $X = MR+1$ ) should be left open circuit.

### DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

### DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2]. When DE is set to OFF (logic "0"), both SEG and COM drivers will become idle and UC1608 will put itself into Sleep mode to conserve power.

When DE is set to ON, UC1608 will first exit from Sleep mode, restore the power ( $V_{LCD}$ ,  $V_{BIAS}$  etc.) and then turn on COM and SEG drivers.

### ALL PIXELS ON (APO)

When set, this flag will force all active SEG drivers to output On signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

### INVERSE (PXV)

When this flag is set to ON, active SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

### SCROLLING

SL register can be used to implement scroll function. Setting SL to a non-zero value N will result in the image being scrolled by N lines.



## ITO LAYOUT CONSIDERATIONS

Since the COM scanning pulses of UC1608 can be as short as 98 $\mu$ S, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

For COG applications, low resistance ITO glass will help reduce SEG signal RC decay, minimize  $V_{DD}$   $V_{SS}$  noise, and ensure sufficient  $V_{DD2}$ ,  $V_{S2}$  supply for on-chip DC-DC converter.

Please ensure to keep  $V_{DD}$  and  $V_{SS}$  under 150 O.

### ITO TRACES FOR COM SIGNALS

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase of COM direction crosstalk.

Please limit the worst case of COM signals RC delay ( $RC_{MAX}$ ) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 5.5\mu S$$

where

- $C_{ROW}$ : LCD loading capacitance of one row of pixels. It can be calculated by  $C_{LCD}/Mux-Rate$ , where  $C_{LCD}$  is the LCD panel capacitance.
- $R_{ROW}$ : ITO resistance over one row of pixels within the active area
- $R_{COM}$ : COM routing resistance from IC to the active area + COM driver output impedance.

(Use worst case values for all calculations)

In addition, please limit the min-max spread of RC decay to be:

$$|RC_{MAX} - RC_{MIN}| < 1.4\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

### ITO TRACES FOR SEG SIGNALS

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase of SEG direction crosstalk.

To minimize crosstalk, please limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.7\mu S$$

where

- $C_{COL}$ : LCD loading capacitance of one pixel column. It can be calculated by  $C_{LCD}/\#\_column$ , where  $C_{LCD}$  is the LCD panel capacitance.
- $R_{COL}$ : ITO resistance over one column of pixels within the active area
- $R_{SEG}$ : SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

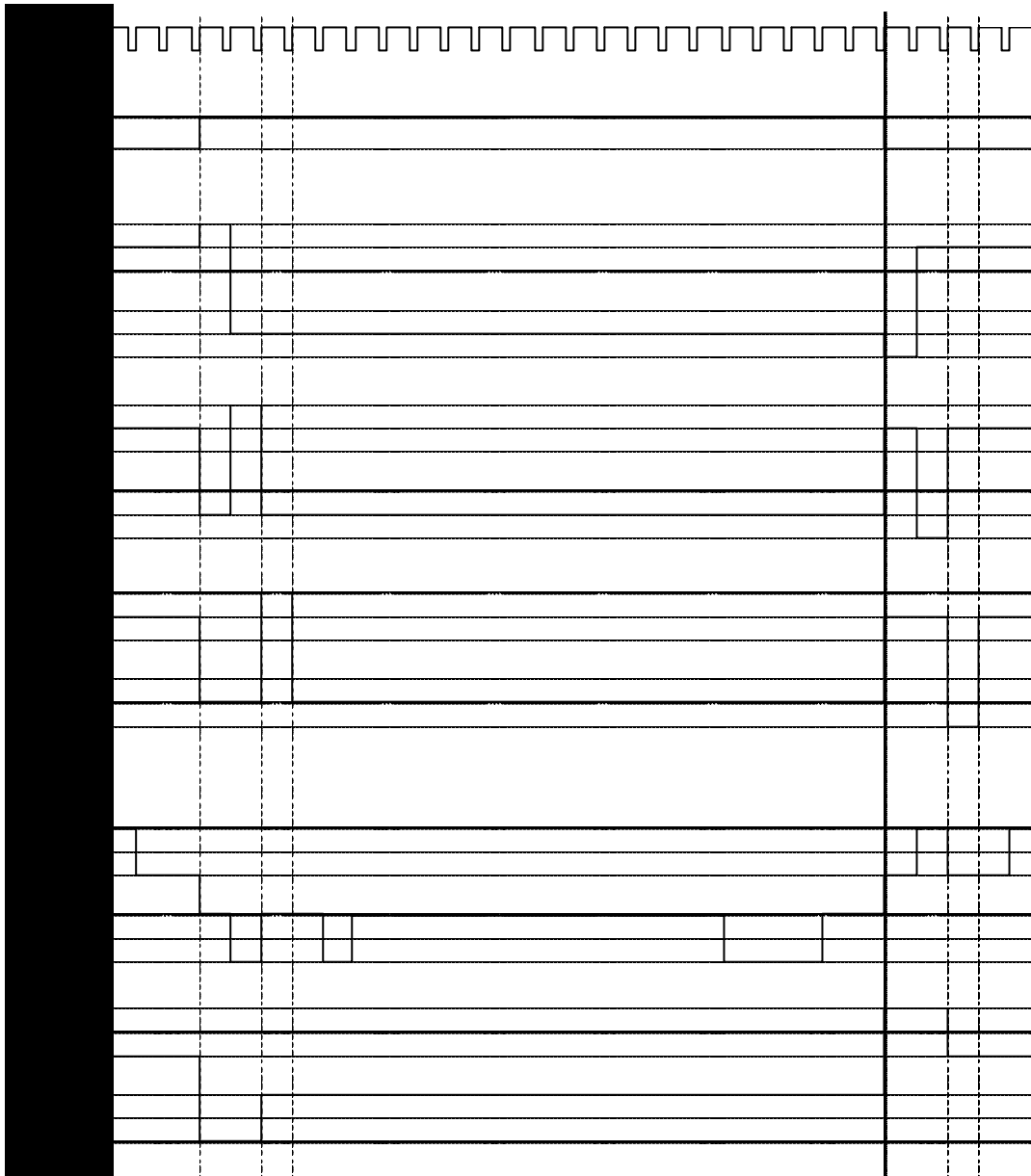


FIGURE 3 : COM and SEG Driving Waveform

## HOST INTERFACE

As summarized in the table below, UC1608 supports two parallel bus protocols, in either 8-bit or 4-bit bus width, and three serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

| Bus Type            |         | 8080            |       | 6800              |       | S8 (4wr)       | S8uc (3wr) | S9 (3wr) |
|---------------------|---------|-----------------|-------|-------------------|-------|----------------|------------|----------|
| Width               |         | 8-bit           | 4-bit | 8-bit             | 4-bit | Serial         |            |          |
| Access              |         | Read/Write      |       |                   |       | Write Only     |            |          |
| Control & Data Pins | BM[1:0] | 10              | 00    | 11                | 01    | 00             |            | 01       |
|                     | D[7:6]  | Data            | 0X    | Data              | 0X    | 10             | 11         | 10       |
|                     | CS      | Chip Select     |       |                   |       |                |            |          |
|                     | CD      | Control/Data    |       |                   |       |                |            |          |
|                     | WR0     | $\overline{WR}$ |       | R/ $\overline{W}$ |       | 0              |            |          |
|                     | WR1     | $\overline{RD}$ |       | EN                |       | 0              |            |          |
|                     | D[5:4]  | Data            | –     | Data              | –     | –              |            |          |
|                     | D[3:0]  | Data            | Data  | Data              | Data  | D0=SCK, D3=SDA |            |          |

\* Connect unused control pins and data bus pins to  $V_{DD}$  or  $V_{SS}$

|          | CS Disable Interface | CS Init bus state | CD 1<=>0 Init bus state | CD 1=>0 init color mapping | RESET Init bus state | RESET init color mapping |
|----------|----------------------|-------------------|-------------------------|----------------------------|----------------------|--------------------------|
| 8-bit    | ✓                    | –                 | –                       | ✓                          | ✓                    | ✓                        |
| 4-bit    | ✓                    | –                 | ✓                       | ✓                          | ✓                    | ✓                        |
| S8 or S9 | ✓                    | ✓                 | –                       | ✓                          | ✓                    | ✓                        |
| S8uc     | ✓                    | –                 | ✓                       | ✓                          | ✓                    | ✓                        |

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- CD refers to CD transitions within valid CS window. CD = 0 means write command or read status.
- CS / CD Sync / RESET can be used to initialize bus state machine (like 4 bits / S8 / S9).
- RESET can be pin reset / soft reset / power on reset.  
CD can be used to initialize the multi-byte input RGB format to/from on-chip SRAM mapping.

**Table 3:** Host interfaces Choices

### PARALLEL INTERFACE

The timing relationship between UC1608 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 4-bit mode, by either *Set CA*, or *Set PA* command, a dummy read cycle need to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

### 8-BIT & 4-BIT BUS OPERATION

UC1608 supports both 8-bit and 4-bit bus width. The bus width is determined by pin BM[1].

4-bit bus operation exactly doubles the clock cycles of 8-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 4-bit mode is reset each time Chip-Select or CD pin changes state.

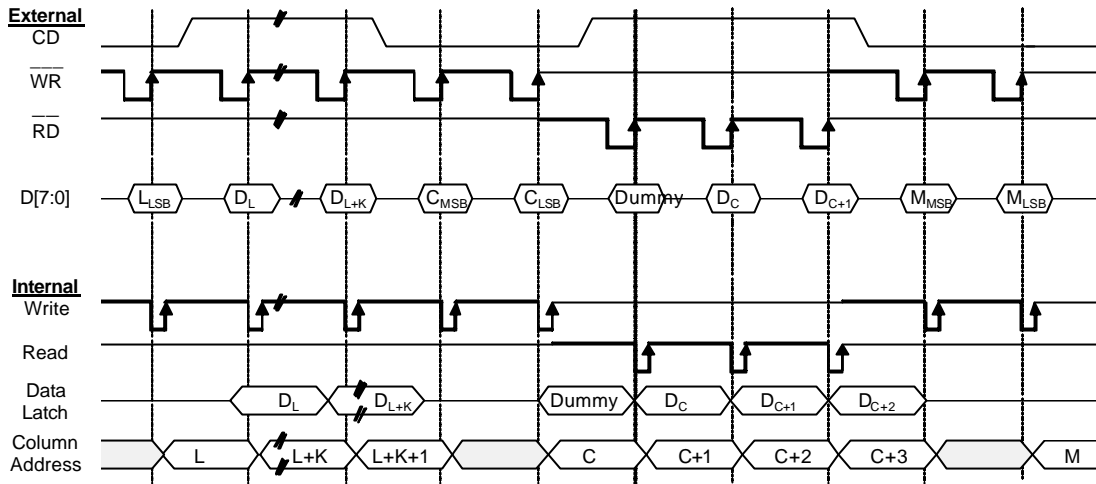


FIGURE 4: 8 bit Parallel Interface & Related Internal Signals

**SERIAL INTERFACE**

UC1608 supports three serial modes, one 4-wire SPI mode (S8), one compact 3/4-wire mode (S8uc) and one 3-wire SPI mode (S9). Bus interface mode is determined by the wiring of the BM[1:0] and D[7:6]. See table on last page for more detail.

of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

**S8 (4-WIRE) INTERFACE**

Only write operations are supported in 4-wire serial mode. Pin CS are used for chip select and bus cycle reset. Pin CD is used to determine the content

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

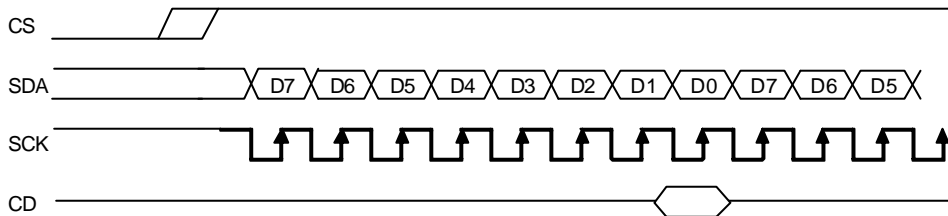


FIGURE 4.a: 4-wire Serial Interface (S8)

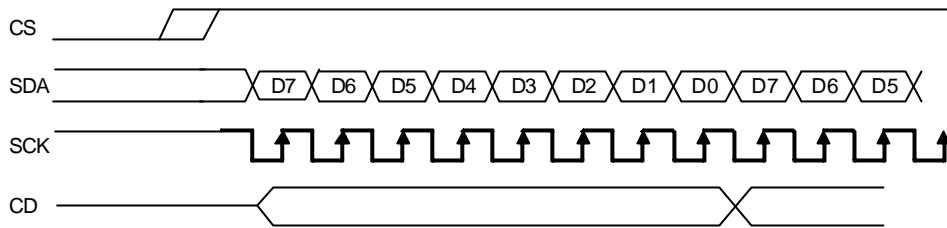


FIGURE 4.b: 3/4-wire Serial Interface (S8uc)

**S8uc (3/4-WIRE) INTERFACE**

Only write operations are supported in this 3/4-wire serial mode. The data format is identical as S8. However, in addition to CS pin, CD pin transitions will also reset the bus cycle in this mode. So, if CS pin are hardwired to enable chip-select, the bus can work properly with only three signal pins.

bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

**S9 (3-WIRE) INTERFACE**

Only write operations are supported in this 3-wire serial mode. Pin CS are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either  $V_{DD}$  or  $V_{SS}$ . The toggle of CS for each byte of data/command is recommended but optional.

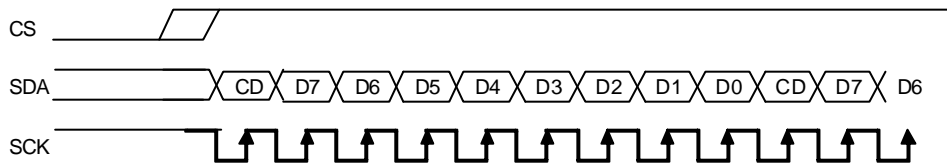
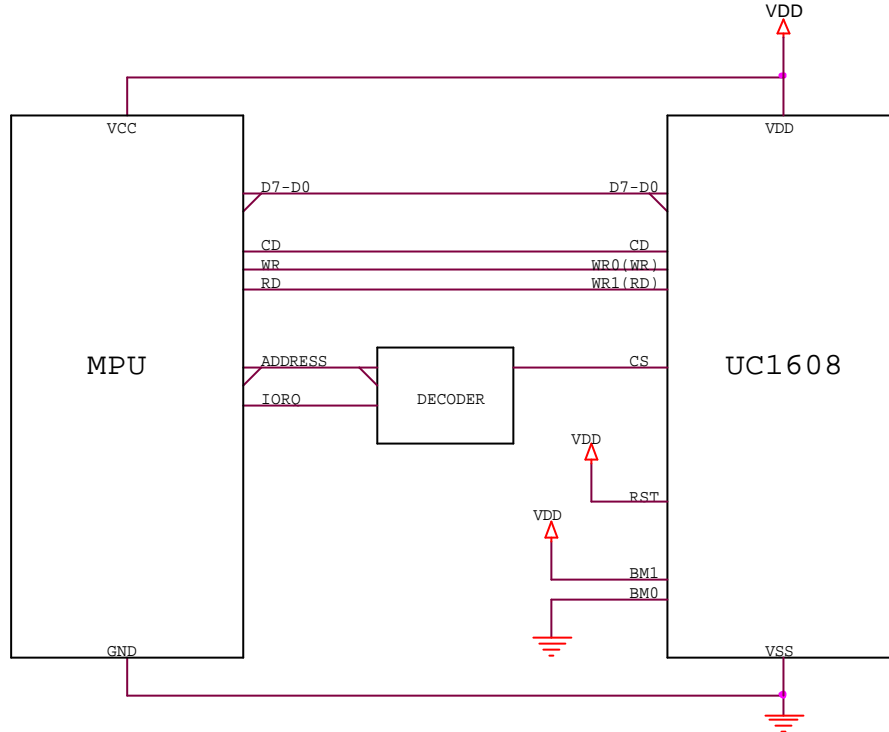
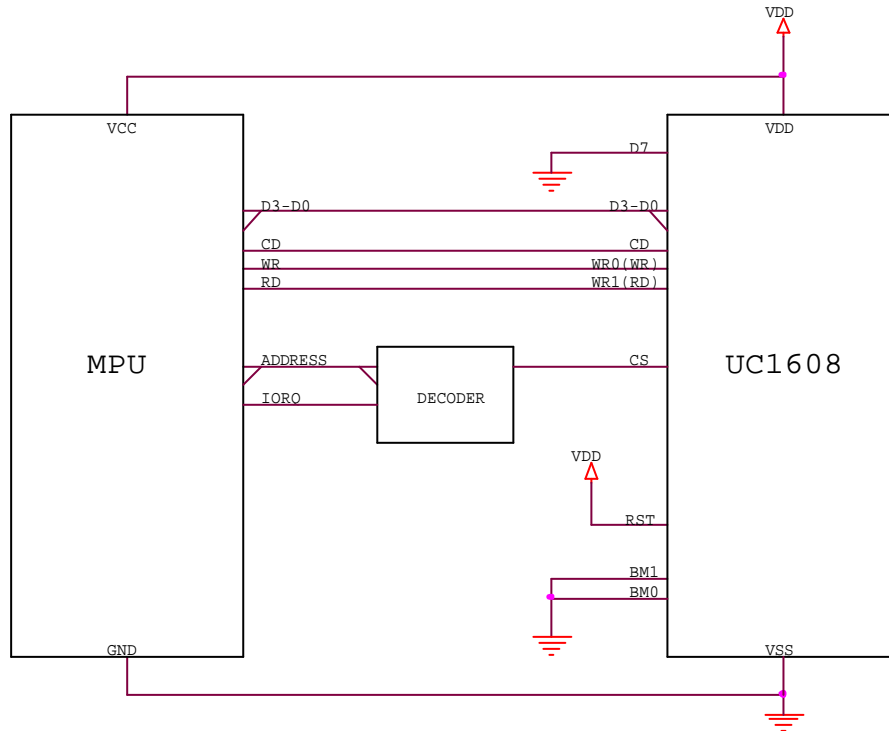


FIGURE 4.c: 3-wire Serial Interface (S9)

**HOST INTERFACE REFERENCE CIRCUIT**



**FIGURE 5: 8080/8bit parallel mode reference circuit**



**FIGURE 6: 8080/4bit parallel mode reference circuit**

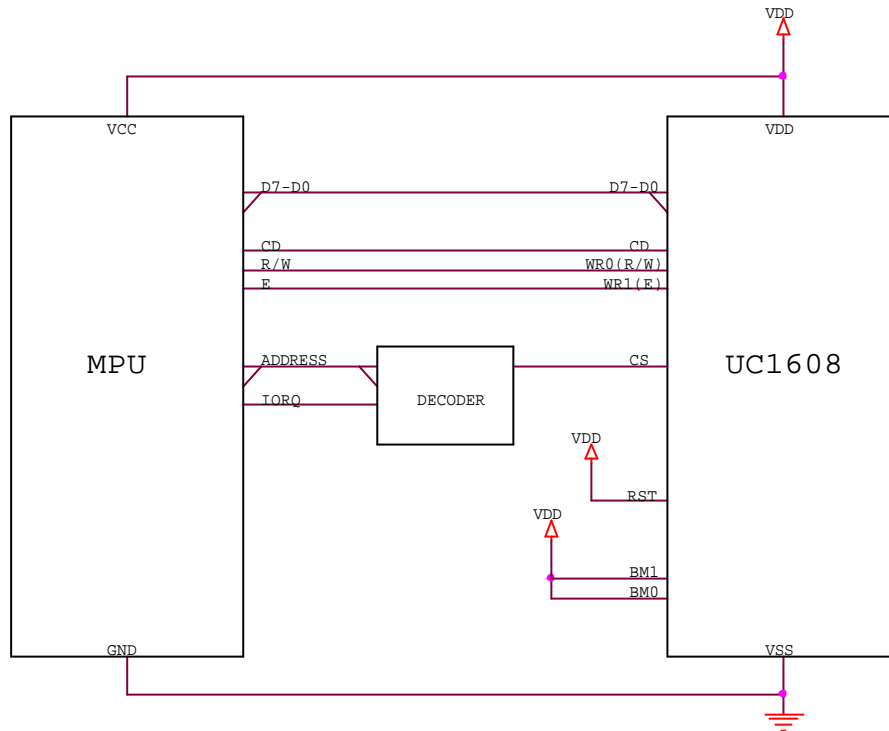


FIGURE 7 : 6800/8bit parallel mode reference circuit

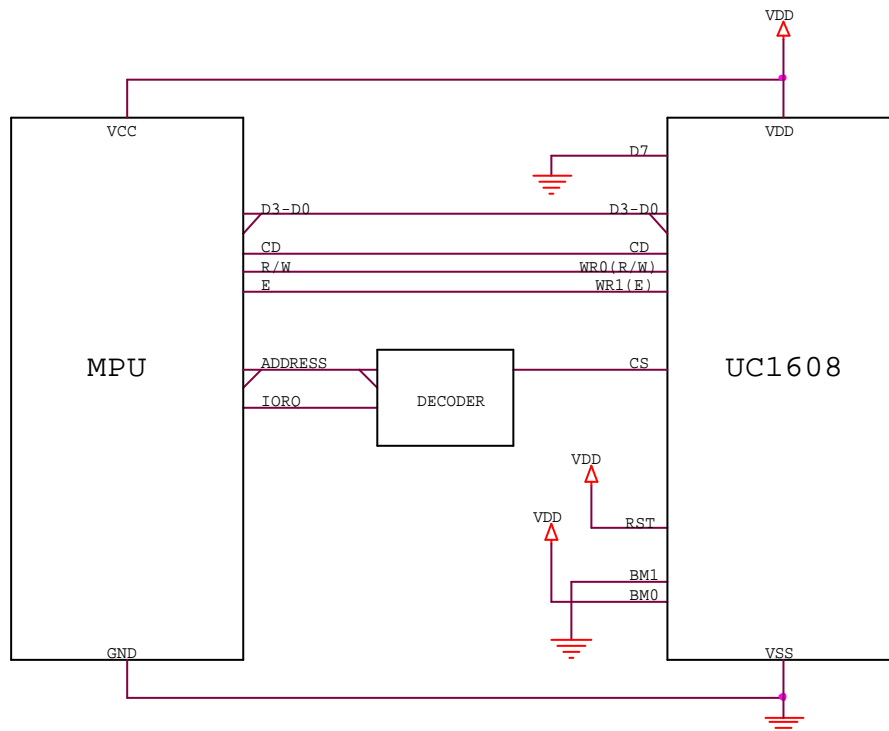


FIGURE 8 : 6800/4bit parallel mode reference circuit

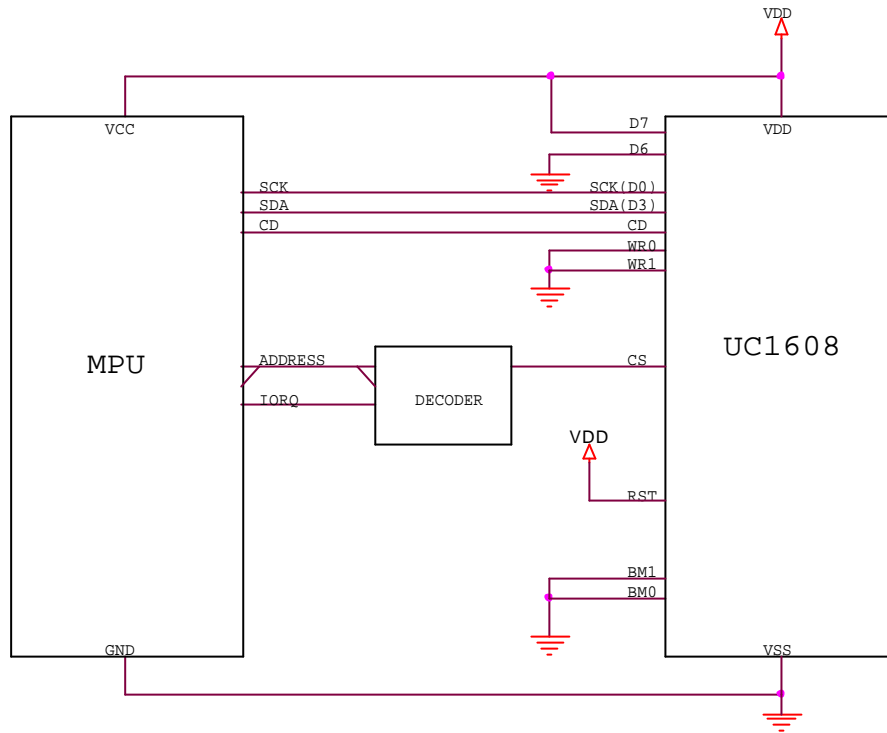


FIGURE 9: 4-Wires SPI (S8) serial mode reference circuit

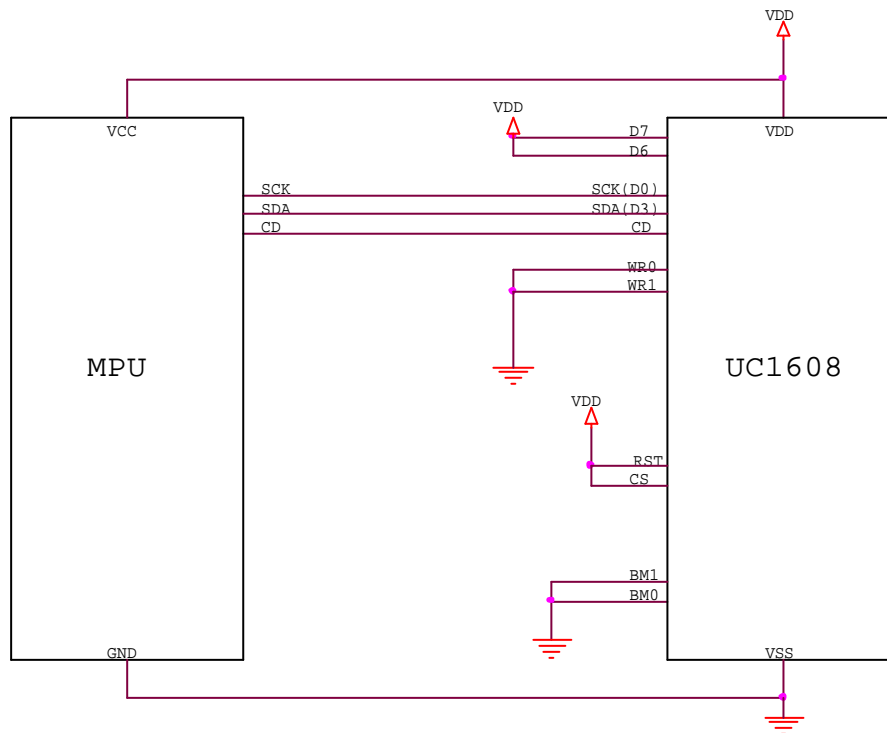


FIGURE 10: 3/4-Wires SPI (S8uc) serial mode reference circuit



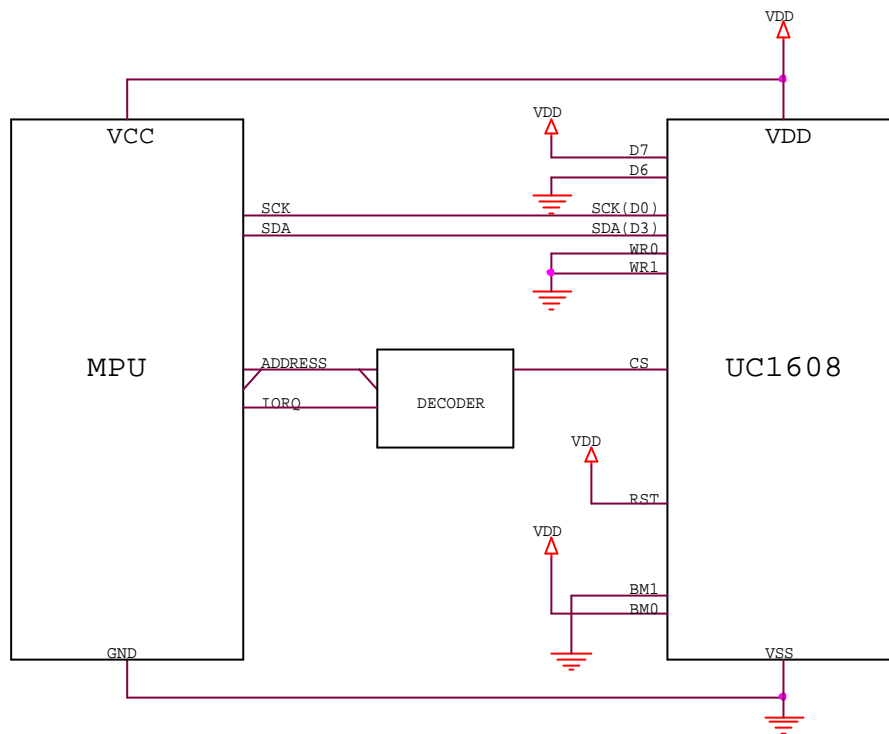


FIGURE 11 : 3-Wires SPI (S9) serial mode reference circuit

**Note**

- RST pin is optional. When RST pin is not used, connect the pin to  $V_{DD}$ .

## DISPLAY DATA RAM

### DATA ORGANIZATION

The display data is 1-bit per pixel and stored in a dual port static RAM (RAM, for Display Data RAM). The RAM size is 128x240 for UC1608. This array of data bits is further organized into pages of 8 bit slices to facilitate parallel bus interface.

When Mirror X (MX, LC[2]) is OFF, the 1<sup>st</sup> column of LCD pixels will correspond to the bits of the first byte of each page, the 2<sup>nd</sup> column of LCD pixels correspond to the bits of the second byte of each page, etc.

### MSB FIRST OR LSB FIRST

There are two options to map D[7:0] to RAM, MSB first (MSF=1), or LSB first (MSF=0), as illustrated in next page.

### DISPLAY DATA RAM ACCESS

The memory used in UC1608 Display Data RAM (RAM) is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

### DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of page (239), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 19), PA will be wrapped around to the other end of RAM and continue.

### MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (239–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

### DISPLAY SCANNING

During each field of display, depending on the setting of MR, COM electrodes will be scanned in a fixed pattern at a rate of

$$(Frame\ Rate \times Mux\ Rate) \text{ rows/second.}$$

During each row period, the signal at the SEG drivers determines the ON/OFF status of the row of pixels being scanned.

### ROW SCANNING

For each field, the scanning starts at COM1 through COMx, where x depends on the setting of MR.

COM electrode scanning (row scanning) orders are not affected by Start Line (SL) or Mirror Y (MY, LC[3]). When MY is 0, the effect of SL having a value *K* is to change the mapping of COM1 to the *K*-th bit slice of data stored in display RAM. Visually, SL having a non-zero value is equivalent to scrolling LCD display up by SL rows.

**RAM ADDRESS GENERATION**

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed Row scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1<sup>st</sup> line period of each field

$$Line = SL$$

Otherwise

$$Line = \text{Mod}(Line+1, 128)$$

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line*+1 reaches 128.

Effects such as page scrolling can be emulated by changing SL dynamically.

**MY IMPLEMENTATION**

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1<sup>st</sup> line period of each field

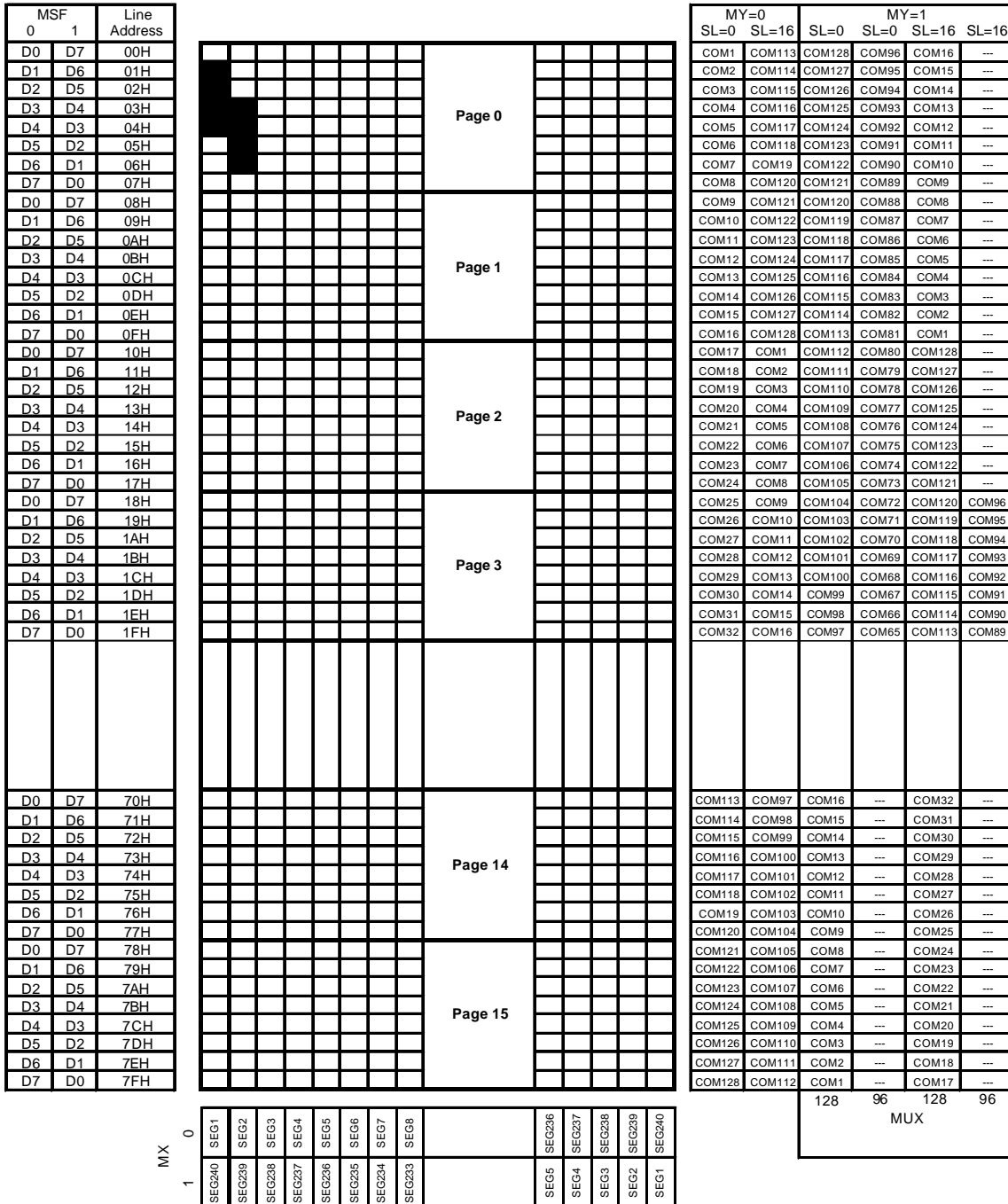
$$Line = \text{Mod}(SL + MUX - 1, 128)$$

where MUX = 96 or 128.

Otherwise

$$Line = \text{Mod}(Line - 1, 128)$$

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.



Example for memory mapping: let MX = 0, MY = 0, SL = 0, MSF = 0, according to the data shown in the above table:

- ⇒ Page 0 SEG 1: 00011110b
- ⇒ Page 0 SEG 2: 01111000b

## RESET & POWER MANAGEMENT

### TYPES OF RESET

UC1608 has two different types of Reset:  
*Power-ON-Reset* and *System-Reset*

*Power-ON-Reset* is performed right after  $V_{DD}$  is connected to power. *Power-On-Reset* will first wait for about 15mS, depending on the time required for  $V_{DD}$  to stabilize, and then trigger the *System Reset*

*System Reset* can also be activated by software command or by connecting RST pin to ground. In the following discussions, Reset means *System Reset*.

### RESET STATUS

When UC1608 enters RESET sequence:

- Operation mode will be "Reset".
  - System Status bits, RS and BZ, will stay 1 until the Reset process is completed *and* a "Display Enable" command is issued. (Issuing a Display Enable command after the Reset process is completed will change status from 1 to 0.
- When BZ=1, the IC will only respond to *Read Status* command; all other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

### OPERATION MODES

UC1608 has three operating modes (OM):  
Reset, Normal, Sleep.

For each mode, the related statuses are as below:

| Mode             | Reset  | Sleep  | Normal |
|------------------|--------|--------|--------|
| OM               | 00     | 10     | 11     |
| Host Interface   | Active | Active | Active |
| Clock            | OFF    | OFF    | ON     |
| LCD Drivers      | OFF    | OFF    | ON     |
| Charge Pump      | OFF    | OFF    | ON     |
| Draining Circuit | ON     | ON     | OFF    |

**Table 4:** Operating Modes

### CHANGING OPERATION MODE

In addition to *Power-ON-Reset*, two commands will initiate OM transitions:

*Set Display Enable*, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

| Action  | Mode   | OM |
|---|--------|----|
| Set Driver Enable to "0"                              | Sleep  | 10 |
| Set Driver Enable to "1"                              | Normal | 11 |
| Reset command or RST pin pulled "L"<br>Power ON reset | Reset  | 00 |

**Table 5:** OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors  $C_{B0}$ ,  $C_{B1}$ , and  $C_L$ . When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1601 consumes very little energy in Sleep mode (typically under 2 $\mu$ A).

### EXITING SLEEP MODE

UC1608 contains internal logic to check whether  $V_{LCD}$  and  $V_{BIAS}$  are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset Mode, COM and SEG drivers will not be activated until UC1608 internal voltage sources are restored to their proper values.

**POWER-UP SEQUENCE**

UC1608 power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 15mS before the CPU starting to issue commands to UC1608. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

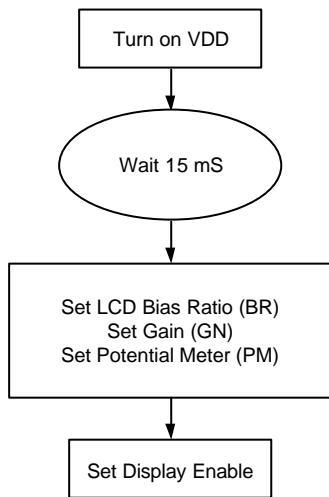


FIGURE 12: Reference Power-Up Sequence

**POWER-DOWN SEQUENCE**

To prevent the charge stored in capacitors  $C_{BX+}$ ,  $C_{BX-}$ , and  $C_L$  from damaging the LCD when  $V_{DD}$  is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K  $\Omega$  for both  $V_{LCD}$  and  $V_{B+}$ . It is recommended to wait  $3 \times RC$  for  $V_{LCD}$  and  $1.5 \times RC$  for  $V_{B+}$ . For example, if  $C_L$  is 10nF, then the draining time required for  $V_{LCD}$  is 1~2mS.

When internal  $V_{LCD}$  is not used, UC1608 will NOT drain  $V_{LCD}$  during RESET. System designers need to make sure external  $V_{LCD}$  source is properly drained off before turning off  $V_{DD}$ .

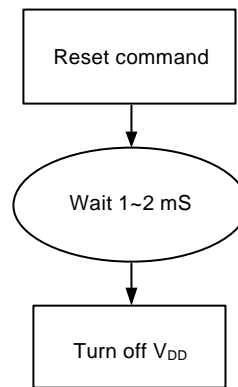


FIGURE 13: Reference Power-Down Sequence

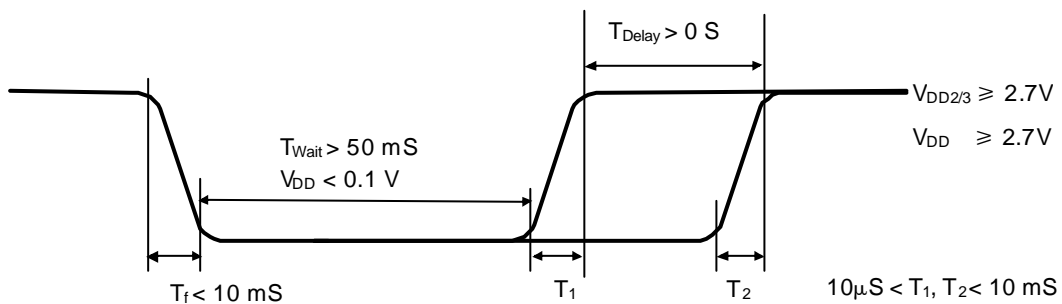


Figure 14: Delay allowance between  $V_{DD}$  and  $V_{DD2/3}$

## SAMPLE POWER COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some “*typical, generic*” scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

Type Required: These items are required

Customized: These item are not necessary if customer parameters are the same as default

Advanced: We recommend new users to skip these commands and use default values.

Optional: These commands depend on what users want to do.

### POWER-UP

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action               | Comments   |
|------|-----|-----|----|----|----|----|----|----|----|----|---------------------------|--|
| R    | –   | –   | –  | –  | –  | –  | –  | –  | –  | –  | Automatic Power-ON-Reset. | Wait 15mS after $V_{DD}$ is ON                                   |
| C    | 0   | 0   | 0  | 0  | 1  | 0  | 0  | #  | #  | #  | (5) Set MR and TC         |  |
| C    | 0   | 0   | 1  | 1  | 0  | 0  | #  | #  | #  | #  | (15) Set LCD Mapping      | Set up LCD specific parameters such as format, MX, MY, MSF, etc. |
| C    | 0   | 0   | 1  | 1  | 1  | 0  | 1  | 0  | #  | #  | (18) Set Bias Ratio       |  |
| R    | 0   | 0   | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | (9) Set Gain & PM         |  |
| C    | 1   | 0   | #  | #  | #  | #  | #  | #  | #  | #  | Write display RAM         | Set up display image   |
|      | .   | .   | .  | .  | .  | .  | .  | .  | .  | .  |                           |  |
|      | .   | .   | .  | .  | .  | .  | .  | .  | .  | .  |                           |  |
|      | 1   | 0   | #  | #  | #  | #  | #  | #  | #  | #  |                           |  |
| R    | 0   | 0   | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 1  | (13) Set Display Enable   |  |

### POWER-DOWN

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action        | Comments                        |
|------|-----|-----|----|----|----|----|----|----|----|----|--------------------|---------------------------------|
| R    | 0   | 0   | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 0  | (16) System Reset  |                                 |
| R    | –   | –   | –  | –  | –  | –  | –  | –  | –  | –  | Draining capacitor | Wait 1~2m S before $V_{DD}$ OFF |

**DISPLAY-OFF**

| Type | C/D | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Chip action              | Comments  |
|------|-----|-----|----|----|----|----|----|----|----|----|--------------------------|---|
| R    | 0   | 0   | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 0  | (13) Set Display Disable |   |
| C    | 1   | 0   | #  | #  | #  | #  | #  | #  | #  | #  | Write display RAM        | Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.) |
|      | .   | .   | .  | .  | .  | .  | .  | .  | .  | .  |                          |   |
|      | 1   | 0   | #  | #  | #  | #  | #  | #  | #  | #  |                          |   |
| R    | 0   | 0   | 1  | 0  | 1  | 0  | 1  | 1  | 1  | 1  | (13) Set Display Enable  |   |

\* This is only recommended for very brief display OFF (under 10mS).

If image becomes unstable use the *Extended Display OFF* approach shown below.



**ABSOLUTE MAXIMUM RATINGS**

In accordance with IEC134, note 1,2 and 3.

| Symbol               | Parameter   | Min. | Max.           | Unit |
|----------------------|---|------|----------------|------|
| $V_{DD}$             | Logic Supply voltage                                | -0.3 | +4.0           | V    |
| $V_{DD2}$            | LCD Generator Supply voltage                        | -0.3 | +4.0           | V    |
| $V_{DD3}$            | Analog Circuit Supply voltage                       | -0.3 | +4.0           | V    |
| $V_{DD2/3} - V_{DD}$ | Voltage difference between $V_{DD}$ and $V_{DD2/3}$ | --   | 1.6            | V    |
| $V_{LCD}$            | LCD Generated voltage (-30°C ~ +80°C)               | -0.3 | +17.0          | V    |
| $V_{IN}$             | Any input voltage                                   | -0.4 | $V_{DD} + 0.5$ | V    |
| $T_{OPR}$            | Operating temperature range                         | -30  | +85            | °C   |
| $T_{STR}$            | Storage temperature                                 | -55  | +125           | °C   |

**Note:**

1.  $V_{DD}$  based on  $V_{SS} = 0V$
2. Stress values listed above may cause permanent damages to the device.

**SPECIFICATIONS**
**DC CHARACTERISTICS**

| Symbol       | Parameter                  | Conditions                         | Min.        | Typ. | Max.        | Unit       |
|--------------|----------------------------|------------------------------------|-------------|------|-------------|------------|
| $V_{DD}$     | Supply for digital circuit |                                    | 2.7         | 2.8  | 3.3         | V          |
| $V_{DD2/3}$  | Supply for bias & pump     |                                    | 2.7         | 2.8  | 3.3         | V          |
| $V_{LCD}$    | Charge pump output         | $V_{DD2/3} \geq 2.7V, 25^{\circ}C$ |             | 12.5 | 16          | V          |
| $V_D$        | LCD data voltage           | $V_{DD2/3} \geq 2.7V, 25^{\circ}C$ |             |      | 1.53        | V          |
| $V_{IL}$     | Input logic LOW            |                                    |             |      | $0.2V_{DD}$ | V          |
| $V_{IH}$     | Input logic HIGH           |                                    | $0.8V_{DD}$ |      |             | V          |
| $V_{OL}$     | Output logic LOW           |                                    |             |      | $0.2V_{DD}$ | V          |
| $V_{OH}$     | Output logic HIGH          |                                    | $0.8V_{DD}$ |      |             | V          |
| $I_{IL}$     | Input leakage current      |                                    |             |      | 1.5         | $\mu A$    |
| $C_{IN}$     | Input capacitance          |                                    |             | 5    | 10          | PF         |
| $C_{OUT}$    | Output capacitance         |                                    |             | 5    | 10          | PF         |
| $R_{O(SEG)}$ | SEG output impedance       | $V_{LCD} = 12.5V$                  |             | 1.5  | 3           | k $\Omega$ |
| $R_{O(COM)}$ | COM output impedance       | $V_{LCD} = 9$                      |             | 1.5  | 3           | k $\Omega$ |
| $f_{LINE}$   | Average frame rate         |                                    | 69          | 75   | --          | Hz         |

**POWER CONSUMPTION**

$V_{DD} = 2.7V$ ,  $V_{DD2/3} = 2.7V$ , Bias Ratio (BR) = 10b, GN = 11b, PM = 000000b,  
 Panel Loading (PL): 26~43nF, MR = 128, Bus mode = 6800,  $C_L = 0.1\mu F$ ,  $C_B = 4.7\mu F$ .  
 All outputs are open circuit.

| Display Pattern | Conditions                   | Typ. ( $\mu A$ ) | Max. ( $\mu A$ ) |
|-----------------|------------------------------|------------------|------------------|
| All-OFF         | Bus = idle                   | 580              | 870              |
| 2-pixel checker | Bus = idle                   | 730              | 1095             |
| --              | Bus = idle (standby current) | --               | 5                |

AC CHARACTERISTICS

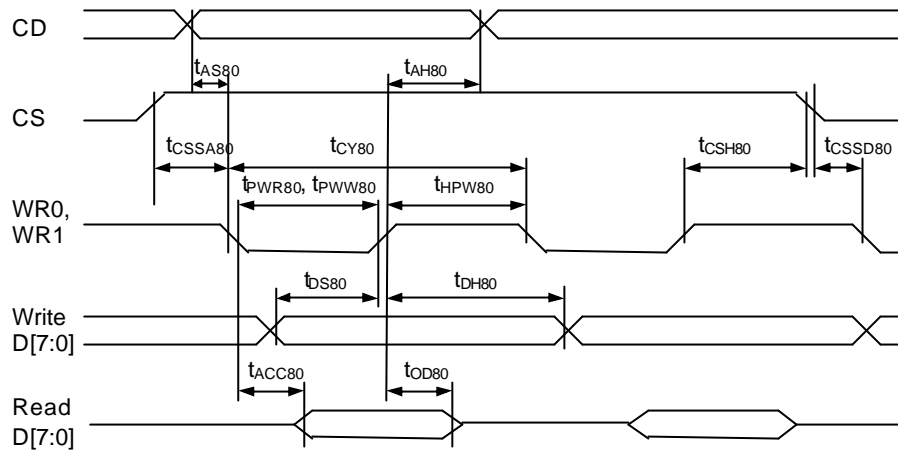


FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

( $2.7V \leq V_{DD} < 3.3V$ ,  $T_a = -30$  to  $+85^\circ C$ )

| Symbol       | Signal   | Description                        | Condition     | Min. | Max. | Units |
|--------------|----------|------------------------------------|---------------|------|------|-------|
| $t_{AS80}$   | CD       | Address setup time                 |               | 0    | -    | nS    |
| $t_{AH80}$   |          | Address hold time                  |               | 20   | -    | nS    |
| $t_{CY80}$   |          | System cycle time                  |               |      |      | nS    |
|              |          | 8 bits bus (read)                  |               | 140  |      |       |
|              |          | (write)                            |               | 140  |      |       |
|              |          | 4 bits bus (read)                  |               | 140  |      |       |
|              |          | (write)                            |               | 140  |      |       |
| $t_{PWR80}$  | WR1      | Pulse width 8 bits (read)          |               | 65   | -    | nS    |
|              |          | 4 bits                             |               | 65   |      |       |
| $t_{PWVW80}$ | WR0      | Pulse width 8 bits (write)         |               | 35   | -    | nS    |
|              |          | 4 bits                             |               | 35   |      |       |
| $t_{HPW80}$  | WR0, WR1 | High pulse width 8 bits bus (read) |               | 65   | -    | nS    |
|              |          | (write)                            |               | 35   |      |       |
|              |          | 4 bits bus (read)                  |               | 65   |      |       |
|              |          | (write)                            |               | 35   |      |       |
| $t_{DS80}$   | D0~D7    | Data setup time                    |               | 30   | -    | nS    |
| $t_{DH80}$   |          | Data hold time                     |               | 20   |      |       |
| $t_{ACC80}$  |          | Read access time                   | $C_L = 100pF$ | -    | 60   | nS    |
| $t_{OD80}$   |          | Output disable time                |               | 12   | 20   |       |
| $t_{SSA80}$  | CS1/CS0  | Chip select setup time             |               | 10   |      | nS    |
| $t_{CSSD80}$ |          |                                    |               | 10   |      |       |
| $t_{CSH80}$  |          |                                    |               | 20   |      |       |

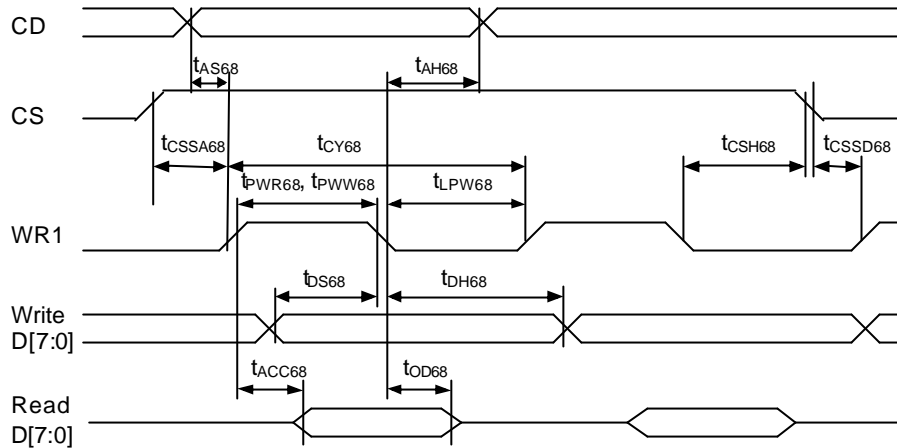


FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

( $2.7V \leq V_{DD} < 3.3V$ ,  $T_a = -30$  to  $+85^\circ C$ )

| Symbol       | Signal  | Description                | Condition     | Min. | Max. | Units |
|--------------|---------|----------------------------|---------------|------|------|-------|
| $t_{AS68}$   | CD      | Address setup time         |               | 0    | -    | nS    |
| $t_{AH68}$   |         | Address hold time          |               | 20   | -    | nS    |
| $T_{CY68}$   |         | System cycle time          |               |      | -    | nS    |
|              |         | 8 bits bus (read)          |               | 140  |      |       |
|              |         | (write)                    |               | 140  |      |       |
|              |         | 4 bits bus (read)          |               | 140  |      |       |
|              |         | (write)                    |               | 140  |      |       |
| $t_{PWR68}$  | WR1     | Pulse width 8 bits (read)  |               | 65   |      |       |
|              |         | 4 bits                     |               | 65   | -    | nS    |
| $t_{PWW68}$  |         | Pulse width 8 bits (write) |               | 35   |      |       |
|              |         | 4 bits                     |               | 35   | -    | nS    |
| $t_{LPW68}$  |         | Low pulse width            |               |      |      |       |
|              |         | 8 bits bus (read)          |               | 65   |      |       |
|              |         | (write)                    |               | 35   |      |       |
|              |         | 4 bits bus (read)          |               | 65   |      |       |
|              |         | (write)                    |               | 35   |      |       |
| $t_{DS68}$   | D0~D7   | Data setup time            |               | 30   |      |       |
| $t_{DH68}$   |         | Data hold time             |               | 20   |      | nS    |
| $t_{ACC68}$  |         | Read access time           | $C_L = 100pF$ | -    | 60   | nS    |
| $t_{OD68}$   |         | Output disable time        |               | 12   | 20   |       |
| $t_{CSSA68}$ | CS1/CS0 | Chip select setup time     |               | 10   |      | nS    |
| $t_{CSSD68}$ |         |                            |               | 10   |      |       |
| $t_{CSh68}$  |         |                            |               | 20   |      |       |

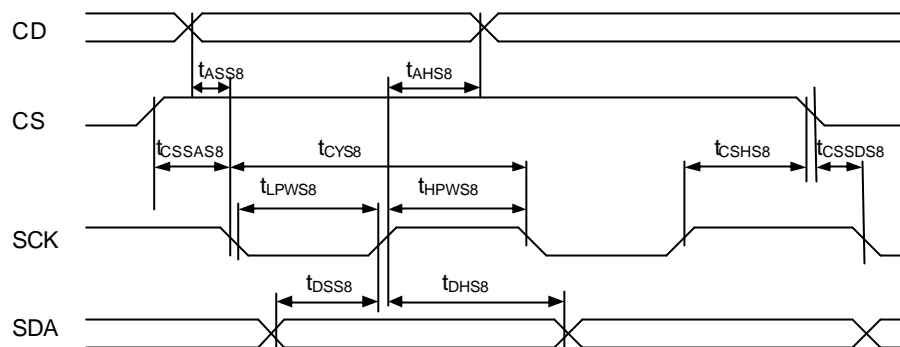
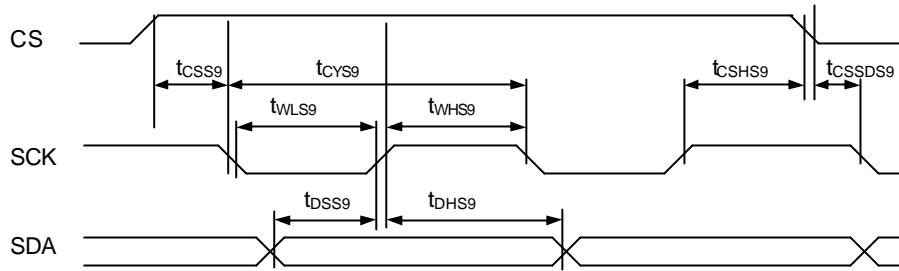


FIGURE 17: Serial Bus Timing Characteristics (for S8)

( $2.7V \leq V_{DD} < 3.3V$ ,  $T_a = -30$  to  $+85^\circ\text{C}$ )

| Symbol       | Signal | Description            | Condition | Min. | Max. | Units |
|--------------|--------|------------------------|-----------|------|------|-------|
| $t_{ASS8}$   | CD     | Address setup time     |           | 0    | –    | nS    |
| $t_{AHS8}$   |        | Address hold time      |           | 20   | –    | nS    |
| $t_{CYS8}$   | SCK    | System cycle time      |           | 140  | –    | nS    |
| $t_{LPWS8}$  |        | Low pulse width        |           | 65   | –    | nS    |
| $t_{HPWS8}$  |        | High pulse width       |           | 65   | –    | nS    |
| $t_{DSS8}$   | SDA    | Data setup time        |           | 30   | –    | nS    |
| $t_{DHS8}$   |        | Data hold time         |           | 20   | –    | nS    |
| $t_{CSSAS8}$ | CS     | Chip select setup time |           | 10   |      | nS    |
| $t_{CSSDS8}$ |        |                        |           | 20   |      |       |
| $t_{CSHS8}$  |        |                        |           | 10   |      |       |



**FIGURE 18:** Serial Bus Timing Characteristics (for S9)

( $2.7V \leq V_{DD} < 3.3V$ ,  $T_a = -30$  to  $+85^\circ C$ )

| Symbol       | Signal | Description            | Condition | Min. | Max. | Units |
|--------------|--------|------------------------|-----------|------|------|-------|
| $t_{CYS9}$   | SCK    | System cycle time      |           | 140  | –    | nS    |
| $t_{LPWS9}$  |        | Low pulse width        |           | 65   | –    | nS    |
| $t_{HPWS9}$  |        | High pulse width       |           | 65   | –    | nS    |
| $t_{DSS9}$   | SDA    | Data setup time        |           | 30   | –    | nS    |
| $t_{DHS9}$   |        | Data hold time         |           | 20   |      |       |
| $t_{CSSAS9}$ | CS     | Chip select setup time |           | 10   |      | nS    |
| $t_{CSSDS9}$ |        |                        |           | 20   |      |       |
| $t_{CSHS9}$  |        |                        |           | 10   |      |       |

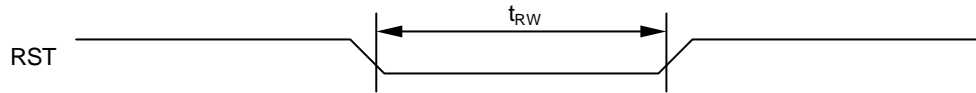


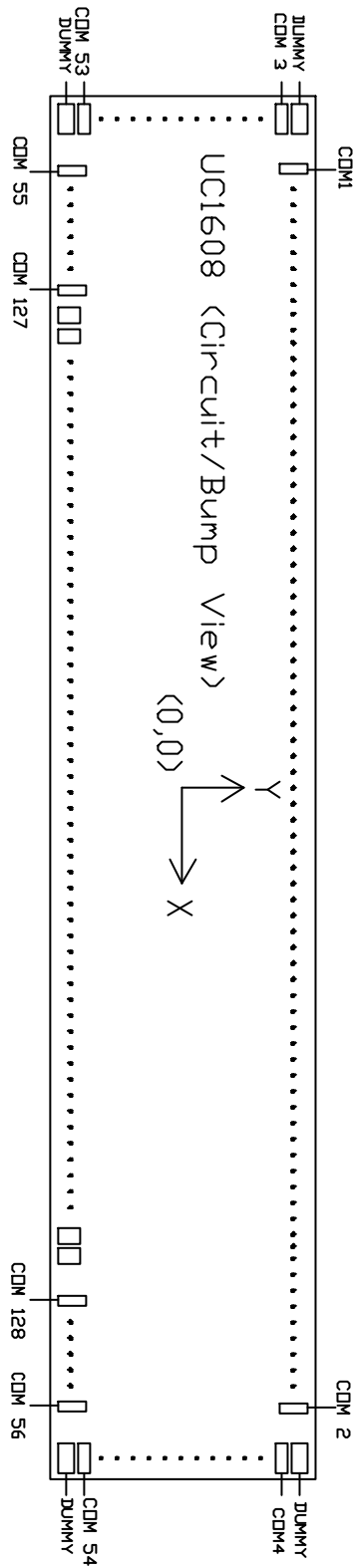
FIGURE 19: Reset Characteristics

( $2.7V \leq V_{DD} < 3.3V$ ,  $T_a = -30$  to  $+85^{\circ}C$ )

| Symbol   | Signal | Description           | Condition | Min. | Max. | Units |
|----------|--------|-----------------------|-----------|------|------|-------|
| $t_{RW}$ | RST    | Reset low pulse width |           | 1000 | –    | nS    |

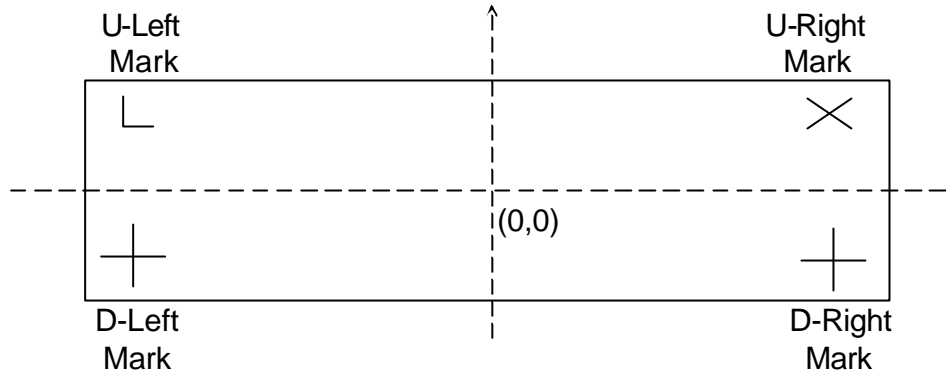
**PHYSICAL DIMENSIONS**

|  |
|--|
| <p><b>DIE SIZE:</b><br/>11480 x 1375 <math>\mu\text{M}^2</math> (Typ.)</p> <p><b>DIE THICKNESS:</b><br/>0.5 mm (Typ.)</p> <p><b>BUMP HEIGHT:</b><br/>17 <math>\pm</math> 1 <math>\mu\text{M}</math> (within die)</p> <p><b>BUMP SIZE:</b><br/>112 x 27 <math>\mu\text{M}^2</math> (Typ.)</p> <p><b>BUMP PITCH:</b><br/>SEG: 45 <math>\mu\text{M}</math> (Typ.)<br/>COM: 45 <math>\mu\text{M}</math> (Typ.)</p> <p><b>BUMP GAP:</b><br/>18 <math>\mu\text{M}</math> (Typ.)</p> <p><b>COORDINATE ORIGIN:</b><br/>Chip center</p> <p><b>PAD REFERENCE:</b><br/>Pad center</p> <p>(Drawing and coordinates are for the Circuit/Bump view.)</p> |
|--|

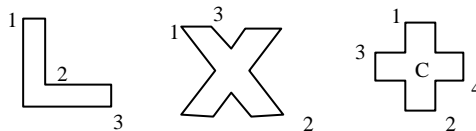




**ALIGNMENT MARK INFORMATION**



**SHAPE OF THE ALIGNMENT MARK:**



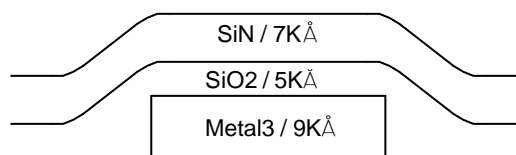
**NOTE :**

Alignment mark is on Metal3 under Passivation.

**COORDINATES :**

|   | U-Left Mark |       | U-Right Mark |       |
|---|-------------|-------|--------------|-------|
|   | X           | Y     | X            | Y     |
| 1 | -5533.5     | 637.1 | 5464.9       | 637.1 |
| 2 | -5517.9     | 626.6 | 5530.0       | 611.0 |
| 3 | -5488.5     | 611.1 | 5490.4       | 637.1 |

|   | D-Left Mark |        | D-Right Mark |        |
|---|-------------|--------|--------------|--------|
|   | X           | Y      | X            | Y      |
| 1 | -5516.5     | -592.1 | 5502.0       | -592.1 |
| 2 | -5505.5     | -637.1 | 5513.0       | -637.1 |
| 3 | -5533.5     | -609.1 | 5485.0       | -609.1 |
| 4 | -5488.5     | -620.1 | 5530.0       | -620.1 |
| C | -5511.0     | -614.6 | 5507.5       | -614.6 |



**FOR NON-OTP PROCESS CROSS-SECTION**

**PAD COORDINATES**

| Pin | Name   | X       | Y      | W     | H     |
|-----|--------|---------|--------|-------|-------|
| 1   | DUMMY  | -5630.3 | 617.0  | 112.0 | 27.0  |
| 2   | COM3   | -5630.3 | 572.0  | 112.0 | 27.0  |
| 3   | COM5   | -5630.3 | 527.0  | 112.0 | 27.0  |
| 4   | COM7   | -5630.3 | 482.0  | 112.0 | 27.0  |
| 5   | COM9   | -5630.3 | 437.0  | 112.0 | 27.0  |
| 6   | COM11  | -5630.3 | 392.0  | 112.0 | 27.0  |
| 7   | COM13  | -5630.3 | 347.0  | 112.0 | 27.0  |
| 8   | COM15  | -5630.3 | 302.0  | 112.0 | 27.0  |
| 9   | COM17  | -5630.3 | 257.0  | 112.0 | 27.0  |
| 10  | COM19  | -5630.3 | 212.0  | 112.0 | 27.0  |
| 11  | COM21  | -5630.3 | 167.0  | 112.0 | 27.0  |
| 12  | COM23  | -5630.3 | 122.0  | 112.0 | 27.0  |
| 13  | COM25  | -5630.3 | 77.0   | 112.0 | 27.0  |
| 14  | COM27  | -5630.3 | 32.0   | 112.0 | 27.0  |
| 15  | COM29  | -5630.3 | -13.0  | 112.0 | 27.0  |
| 16  | COM31  | -5630.3 | -58.0  | 112.0 | 27.0  |
| 17  | COM33  | -5630.3 | -103.0 | 112.0 | 27.0  |
| 18  | COM35  | -5630.3 | -148.0 | 112.0 | 27.0  |
| 19  | COM37  | -5630.3 | -193.0 | 112.0 | 27.0  |
| 20  | COM39  | -5630.3 | -238.0 | 112.0 | 27.0  |
| 21  | COM41  | -5630.3 | -283.0 | 112.0 | 27.0  |
| 22  | COM43  | -5630.3 | -328.0 | 112.0 | 27.0  |
| 23  | COM45  | -5630.3 | -373.0 | 112.0 | 27.0  |
| 24  | COM47  | -5630.3 | -418.0 | 112.0 | 27.0  |
| 25  | COM49  | -5630.3 | -463.0 | 112.0 | 27.0  |
| 26  | COM51  | -5630.3 | -508.0 | 112.0 | 27.0  |
| 27  | COM53  | -5630.3 | -553.0 | 112.0 | 27.0  |
| 28  | DUMMY  | -5630.3 | -598.0 | 112.0 | 27.0  |
| 29  | COM55  | -5422.5 | -577.6 | 27.0  | 112.0 |
| 30  | COM57  | -5377.5 | -577.6 | 27.0  | 112.0 |
| 31  | COM59  | -5332.5 | -577.6 | 27.0  | 112.0 |
| 32  | COM61  | -5287.5 | -577.6 | 27.0  | 112.0 |
| 33  | COM63  | -5242.5 | -577.6 | 27.0  | 112.0 |
| 34  | COM65  | -5197.5 | -577.6 | 27.0  | 112.0 |
| 35  | COM67  | -5152.5 | -577.6 | 27.0  | 112.0 |
| 36  | COM69  | -5107.5 | -577.6 | 27.0  | 112.0 |
| 37  | COM71  | -5062.5 | -577.6 | 27.0  | 112.0 |
| 38  | COM73  | -5017.5 | -577.6 | 27.0  | 112.0 |
| 39  | COM75  | -4972.5 | -577.6 | 27.0  | 112.0 |
| 40  | COM77  | -4927.5 | -577.6 | 27.0  | 112.0 |
| 41  | COM79  | -4882.5 | -577.6 | 27.0  | 112.0 |
| 42  | COM81  | -4837.5 | -577.6 | 27.0  | 112.0 |
| 43  | COM83  | -4792.5 | -577.6 | 27.0  | 112.0 |
| 44  | COM85  | -4747.5 | -577.6 | 27.0  | 112.0 |
| 45  | COM87  | -4702.5 | -577.6 | 27.0  | 112.0 |
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| 47  | COM91  | -4612.5 | -577.6 | 27.0  | 112.0 |
| 48  | COM93  | -4567.5 | -577.6 | 27.0  | 112.0 |
| 49  | COM95  | -4522.5 | -577.6 | 27.0  | 112.0 |
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| 53  | COM103 | -4342.5 | -577.6 | 27.0  | 112.0 |
| 54  | COM105 | -4297.5 | -577.6 | 27.0  | 112.0 |
| 55  | COM107 | -4252.5 | -577.6 | 27.0  | 112.0 |
| 56  | COM109 | -4207.5 | -577.6 | 27.0  | 112.0 |
| 57  | COM111 | -4162.5 | -577.6 | 27.0  | 112.0 |
| 58  | COM113 | -4117.5 | -577.6 | 27.0  | 112.0 |
| 59  | COM115 | -4072.5 | -577.6 | 27.0  | 112.0 |
| 60  | COM117 | -4027.5 | -577.6 | 27.0  | 112.0 |
| 61  | COM119 | -3982.5 | -577.6 | 27.0  | 112.0 |
| 62  | COM121 | -3937.5 | -577.6 | 27.0  | 112.0 |
| 63  | COM123 | -3892.5 | -577.6 | 27.0  | 112.0 |

| Pin | Name    | X       | Y      | W    | H     |
|-----|---------|---------|--------|------|-------|
| 64  | COM125  | -3847.5 | -577.6 | 27.0 | 112.0 |
| 65  | COM127  | -3802.5 | -577.6 | 27.0 | 112.0 |
| 66  | BM1     | -3728.6 | -591.1 | 52.0 | 85.0  |
| 67  | BMD     | -3653.8 | -591.1 | 52.0 | 85.0  |
| 68  | VDDX    | -3583.2 | -591.1 | 52.0 | 85.0  |
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| 80  | D6      | -2714.2 | -591.1 | 52.0 | 85.0  |
| 81  | D7      | -2644.2 | -591.1 | 52.0 | 85.0  |
| 82  | VDD     | -2573.3 | -591.1 | 52.0 | 85.0  |
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| 86  | VDD     | -2293.3 | -591.1 | 52.0 | 85.0  |
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| 89  | VDD2    | -1642.3 | -591.1 | 52.0 | 85.0  |
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| 91  | VDD2    | -1502.3 | -591.1 | 52.0 | 85.0  |
| 92  | VDD3    | -1228.4 | -591.1 | 52.0 | 85.0  |
| 93  | VDD3    | -1158.2 | -591.1 | 52.0 | 85.0  |
| 94  | VDD3    | -1088.2 | -591.1 | 52.0 | 85.0  |
| 95  | VSS2    | -1018.2 | -591.1 | 52.0 | 85.0  |
| 96  | VSS2    | -948.2  | -591.1 | 52.0 | 85.0  |
| 97  | VSS2    | -878.2  | -591.1 | 52.0 | 85.0  |
| 98  | VSS2    | -808.2  | -591.1 | 52.0 | 85.0  |
| 99  | VSS2    | -738.2  | -591.1 | 52.0 | 85.0  |
| 100 | VSS     | -556.2  | -591.1 | 52.0 | 85.0  |
| 101 | VSS     | -486.2  | -591.1 | 52.0 | 85.0  |
| 102 | VSS     | -416.2  | -591.1 | 52.0 | 85.0  |
| 103 | VSS     | -346.2  | -591.1 | 52.0 | 85.0  |
| 104 | VBIAS   | -276.2  | -591.1 | 52.0 | 85.0  |
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| 108 | VLCDIN  | 402.1   | -591.1 | 52.0 | 85.0  |
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| 110 | TP2     | 732.5   | -591.1 | 52.0 | 85.0  |
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| 122 | TST4    | 1956.3  | -591.1 | 52.0 | 85.0  |
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| 126 | VB1+    | 2616.6  | -591.1 | 52.0 | 85.0  |

| Pin | Name   | X      | Y      | W     | H     |
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| 129 | VB1+   | 2826.6 | -591.1 | 52.0  | 85.0  |
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| 131 | TST3   | 3177.7 | -591.1 | 52.0  | 85.0  |
| 132 | VB1-   | 3394.9 | -591.1 | 52.0  | 85.0  |
| 133 | VB1-   | 3465.1 | -591.1 | 52.0  | 85.0  |
| 134 | VB1-   | 3535.1 | -591.1 | 52.0  | 85.0  |
| 135 | VB1-   | 3605.1 | -591.1 | 52.0  | 85.0  |
| 136 | VB1-   | 3675.1 | -591.1 | 52.0  | 85.0  |
| 137 | VB1-   | 3745.1 | -591.1 | 52.0  | 85.0  |
| 138 | COM128 | 3802.5 | -577.6 | 27.0  | 112.0 |
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| 166 | COM72  | 5062.5 | -577.6 | 27.0  | 112.0 |
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| 172 | COM60  | 5332.5 | -577.6 | 27.0  | 112.0 |
| 173 | COM58  | 5377.5 | -577.6 | 27.0  | 112.0 |
| 174 | COM56  | 5422.5 | -577.6 | 27.0  | 112.0 |
| 175 | DUMMY  | 5630.3 | -598.0 | 112.0 | 27.0  |
| 176 | COM54  | 5630.3 | -553.0 | 112.0 | 27.0  |
| 177 | COM52  | 5630.3 | -508.0 | 112.0 | 27.0  |
| 178 | COM50  | 5630.3 | -463.0 | 112.0 | 27.0  |
| 179 | COM48  | 5630.3 | -418.0 | 112.0 | 27.0  |
| 180 | COM46  | 5630.3 | -373.0 | 112.0 | 27.0  |
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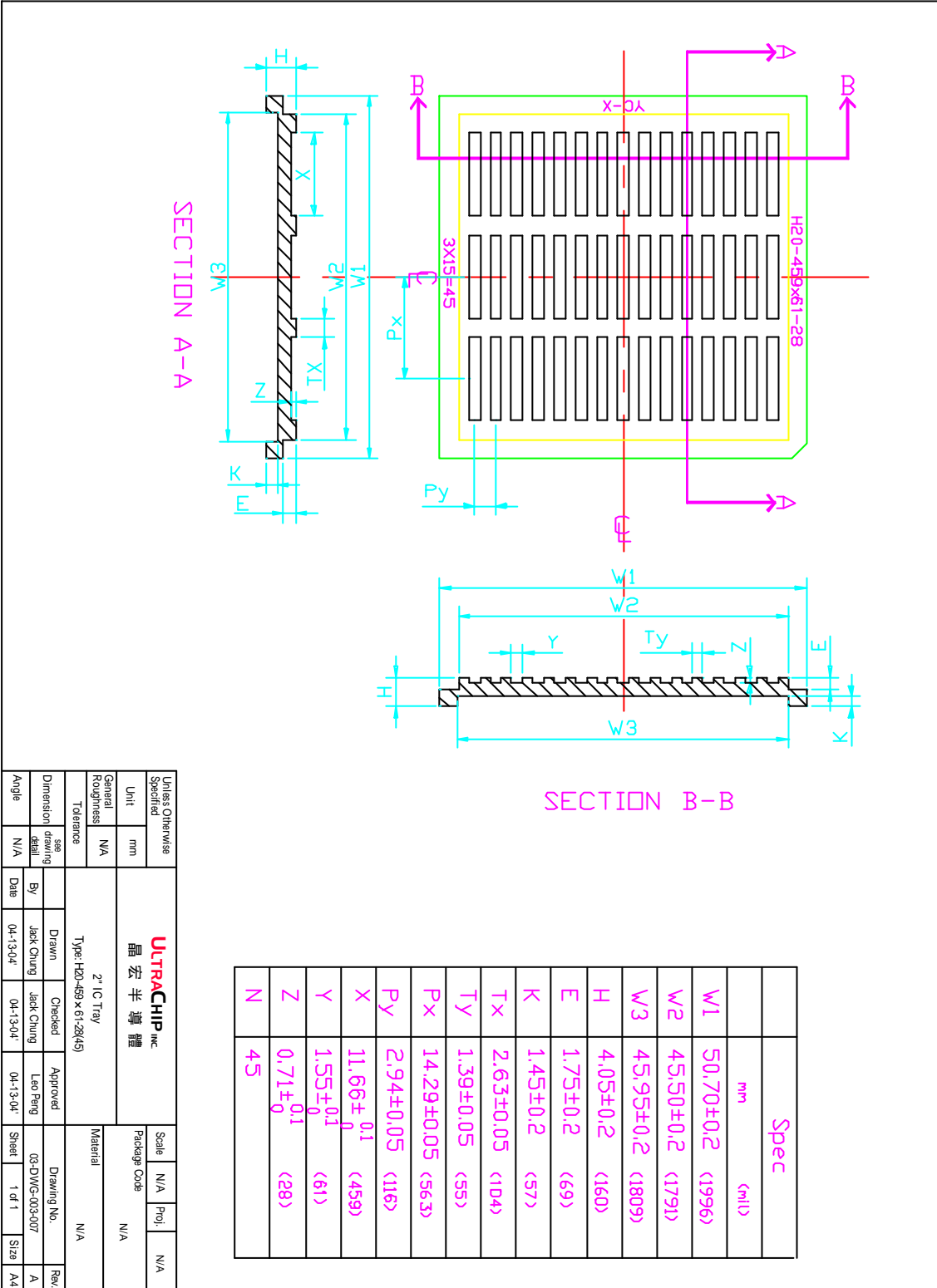
| Pin | Name  | X      | Y     | W     | H     |
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| 193 | COM20 | 5630.3 | 212.0 | 112.0 | 27.0  |
| 194 | COM18 | 5630.3 | 257.0 | 112.0 | 27.0  |
| 195 | COM16 | 5630.3 | 302.0 | 112.0 | 27.0  |
| 196 | COM14 | 5630.3 | 347.0 | 112.0 | 27.0  |
| 197 | COM12 | 5630.3 | 392.0 | 112.0 | 27.0  |
| 198 | COM10 | 5630.3 | 437.0 | 112.0 | 27.0  |
| 199 | COM8  | 5630.3 | 482.0 | 112.0 | 27.0  |
| 200 | COM6  | 5630.3 | 527.0 | 112.0 | 27.0  |
| 201 | COM4  | 5630.3 | 572.0 | 112.0 | 27.0  |
| 202 | DUMMY | 5630.3 | 617.0 | 112.0 | 27.0  |
| 203 | COM2  | 5422.5 | 577.6 | 27.0  | 112.0 |
| 204 | SEG1  | 5377.5 | 577.6 | 27.0  | 112.0 |
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| 206 | SEG3  | 5287.5 | 577.6 | 27.0  | 112.0 |
| 207 | SEG4  | 5242.5 | 577.6 | 27.0  | 112.0 |
| 208 | SEG5  | 5197.5 | 577.6 | 27.0  | 112.0 |
| 209 | SEG6  | 5152.5 | 577.6 | 27.0  | 112.0 |
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| 213 | SEG10 | 4972.5 | 577.6 | 27.0  | 112.0 |
| 214 | SEG11 | 4927.5 | 577.6 | 27.0  | 112.0 |
| 215 | SEG12 | 4882.5 | 577.6 | 27.0  | 112.0 |
| 216 | SEG13 | 4837.5 | 577.6 | 27.0  | 112.0 |
| 217 | SEG14 | 4792.5 | 577.6 | 27.0  | 112.0 |
| 218 | SEG15 | 4747.5 | 577.6 | 27.0  | 112.0 |
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| 222 | SEG19 | 4567.5 | 577.6 | 27.0  | 112.0 |
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| 225 | SEG22 | 4432.5 | 577.6 | 27.0  | 112.0 |
| 226 | SEG23 | 4387.5 | 577.6 | 27.0  | 112.0 |
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| 237 | SEG34 | 3892.5 | 577.6 | 27.0  | 112.0 |
| 238 | SEG35 | 3847.5 | 577.6 | 27.0  | 112.0 |
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| 240 | SEG37 | 3757.5 | 577.6 | 27.0  | 112.0 |
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| 255 | SEG52 | 3082.5 | 577.6 | 27.0  | 112.0 |
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| Pin | Name   | X      | Y     | W    | H     |
|-----|--------|--------|-------|------|-------|
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| 268 | SEG65  | 2497.5 | 577.6 | 27.0 | 112.0 |
| 269 | SEG66  | 2452.5 | 577.6 | 27.0 | 112.0 |
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| 271 | SEG68  | 2362.5 | 577.6 | 27.0 | 112.0 |
| 272 | SEG69  | 2317.5 | 577.6 | 27.0 | 112.0 |
| 273 | SEG70  | 2272.5 | 577.6 | 27.0 | 112.0 |
| 274 | SEG71  | 2227.5 | 577.6 | 27.0 | 112.0 |
| 275 | SEG72  | 2182.5 | 577.6 | 27.0 | 112.0 |
| 276 | SEG73  | 2137.5 | 577.6 | 27.0 | 112.0 |
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| 283 | SEG80  | 1822.5 | 577.6 | 27.0 | 112.0 |
| 284 | SEG81  | 1777.5 | 577.6 | 27.0 | 112.0 |
| 285 | SEG82  | 1732.5 | 577.6 | 27.0 | 112.0 |
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| 287 | SEG84  | 1642.5 | 577.6 | 27.0 | 112.0 |
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| 293 | SEG90  | 1372.5 | 577.6 | 27.0 | 112.0 |
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| 299 | SEG96  | 1102.5 | 577.6 | 27.0 | 112.0 |
| 300 | SEG97  | 1057.5 | 577.6 | 27.0 | 112.0 |
| 301 | SEG98  | 1012.5 | 577.6 | 27.0 | 112.0 |
| 302 | SEG99  | 967.5  | 577.6 | 27.0 | 112.0 |
| 303 | SEG100 | 922.5  | 577.6 | 27.0 | 112.0 |
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| 305 | SEG102 | 832.5  | 577.6 | 27.0 | 112.0 |
| 306 | SEG103 | 787.5  | 577.6 | 27.0 | 112.0 |
| 307 | SEG104 | 742.5  | 577.6 | 27.0 | 112.0 |
| 308 | SEG105 | 697.5  | 577.6 | 27.0 | 112.0 |
| 309 | SEG106 | 652.5  | 577.6 | 27.0 | 112.0 |
| 310 | SEG107 | 607.5  | 577.6 | 27.0 | 112.0 |
| 311 | SEG108 | 562.5  | 577.6 | 27.0 | 112.0 |
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| 314 | SEG111 | 427.5  | 577.6 | 27.0 | 112.0 |
| 315 | SEG112 | 382.5  | 577.6 | 27.0 | 112.0 |
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| Pin | Name   | X       | Y     | W    | H     |
|-----|--------|---------|-------|------|-------|
| 322 | SEG119 | 67.5    | 577.6 | 27.0 | 112.0 |
| 323 | SEG120 | 22.5    | 577.6 | 27.0 | 112.0 |
| 324 | SEG121 | -22.5   | 577.6 | 27.0 | 112.0 |
| 325 | SEG122 | -67.5   | 577.6 | 27.0 | 112.0 |
| 326 | SEG123 | -112.5  | 577.6 | 27.0 | 112.0 |
| 327 | SEG124 | -157.5  | 577.6 | 27.0 | 112.0 |
| 328 | SEG125 | -202.5  | 577.6 | 27.0 | 112.0 |
| 329 | SEG126 | -247.5  | 577.6 | 27.0 | 112.0 |
| 330 | SEG127 | -292.5  | 577.6 | 27.0 | 112.0 |
| 331 | SEG128 | -337.5  | 577.6 | 27.0 | 112.0 |
| 332 | SEG129 | -382.5  | 577.6 | 27.0 | 112.0 |
| 333 | SEG130 | -427.5  | 577.6 | 27.0 | 112.0 |
| 334 | SEG131 | -472.5  | 577.6 | 27.0 | 112.0 |
| 335 | SEG132 | -517.5  | 577.6 | 27.0 | 112.0 |
| 336 | SEG133 | -562.5  | 577.6 | 27.0 | 112.0 |
| 337 | SEG134 | -607.5  | 577.6 | 27.0 | 112.0 |
| 338 | SEG135 | -652.5  | 577.6 | 27.0 | 112.0 |
| 339 | SEG136 | -697.5  | 577.6 | 27.0 | 112.0 |
| 340 | SEG137 | -742.5  | 577.6 | 27.0 | 112.0 |
| 341 | SEG138 | -787.5  | 577.6 | 27.0 | 112.0 |
| 342 | SEG139 | -832.5  | 577.6 | 27.0 | 112.0 |
| 343 | SEG140 | -877.5  | 577.6 | 27.0 | 112.0 |
| 344 | SEG141 | -922.5  | 577.6 | 27.0 | 112.0 |
| 345 | SEG142 | -967.5  | 577.6 | 27.0 | 112.0 |
| 346 | SEG143 | -1012.5 | 577.6 | 27.0 | 112.0 |
| 347 | SEG144 | -1057.5 | 577.6 | 27.0 | 112.0 |
| 348 | SEG145 | -1102.5 | 577.6 | 27.0 | 112.0 |
| 349 | SEG146 | -1147.5 | 577.6 | 27.0 | 112.0 |
| 350 | SEG147 | -1192.5 | 577.6 | 27.0 | 112.0 |
| 351 | SEG148 | -1237.5 | 577.6 | 27.0 | 112.0 |
| 352 | SEG149 | -1282.5 | 577.6 | 27.0 | 112.0 |
| 353 | SEG150 | -1327.5 | 577.6 | 27.0 | 112.0 |
| 354 | SEG151 | -1372.5 | 577.6 | 27.0 | 112.0 |
| 355 | SEG152 | -1417.5 | 577.6 | 27.0 | 112.0 |
| 356 | SEG153 | -1462.5 | 577.6 | 27.0 | 112.0 |
| 357 | SEG154 | -1507.5 | 577.6 | 27.0 | 112.0 |
| 358 | SEG155 | -1552.5 | 577.6 | 27.0 | 112.0 |
| 359 | SEG156 | -1597.5 | 577.6 | 27.0 | 112.0 |
| 360 | SEG157 | -1642.5 | 577.6 | 27.0 | 112.0 |
| 361 | SEG158 | -1687.5 | 577.6 | 27.0 | 112.0 |
| 362 | SEG159 | -1732.5 | 577.6 | 27.0 | 112.0 |
| 363 | SEG160 | -1777.5 | 577.6 | 27.0 | 112.0 |
| 364 | SEG161 | -1822.5 | 577.6 | 27.0 | 112.0 |
| 365 | SEG162 | -1867.5 | 577.6 | 27.0 | 112.0 |
| 366 | SEG163 | -1912.5 | 577.6 | 27.0 | 112.0 |
| 367 | SEG164 | -1957.5 | 577.6 | 27.0 | 112.0 |
| 368 | SEG165 | -2002.5 | 577.6 | 27.0 | 112.0 |
| 369 | SEG166 | -2047.5 | 577.6 | 27.0 | 112.0 |
| 370 | SEG167 | -2092.5 | 577.6 | 27.0 | 112.0 |
| 371 | SEG168 | -2137.5 | 577.6 | 27.0 | 112.0 |
| 372 | SEG169 | -2182.5 | 577.6 | 27.0 | 112.0 |
| 373 | SEG170 | -2227.5 | 577.6 | 27.0 | 112.0 |
| 374 | SEG171 | -2272.5 | 577.6 | 27.0 | 112.0 |
| 375 | SEG172 | -2317.5 | 577.6 | 27.0 | 112.0 |
| 376 | SEG173 | -2362.5 | 577.6 | 27.0 | 112.0 |
| 377 | SEG174 | -2407.5 | 577.6 | 27.0 | 112.0 |
| 378 | SEG175 | -2452.5 | 577.6 | 27.0 | 112.0 |
| 379 | SEG176 | -2497.5 | 577.6 | 27.0 | 112.0 |
| 380 | SEG177 | -2542.5 | 577.6 | 27.0 | 112.0 |
| 381 | SEG178 | -2587.5 | 577.6 | 27.0 | 112.0 |
| 382 | SEG179 | -2632.5 | 577.6 | 27.0 | 112.0 |
| 383 | SEG180 | -2677.5 | 577.6 | 27.0 | 112.0 |
| 384 | SEG181 | -2722.5 | 577.6 | 27.0 | 112.0 |
| 385 | SEG182 | -2767.5 | 577.6 | 27.0 | 112.0 |
| 386 | SEG183 | -2812.5 | 577.6 | 27.0 | 112.0 |

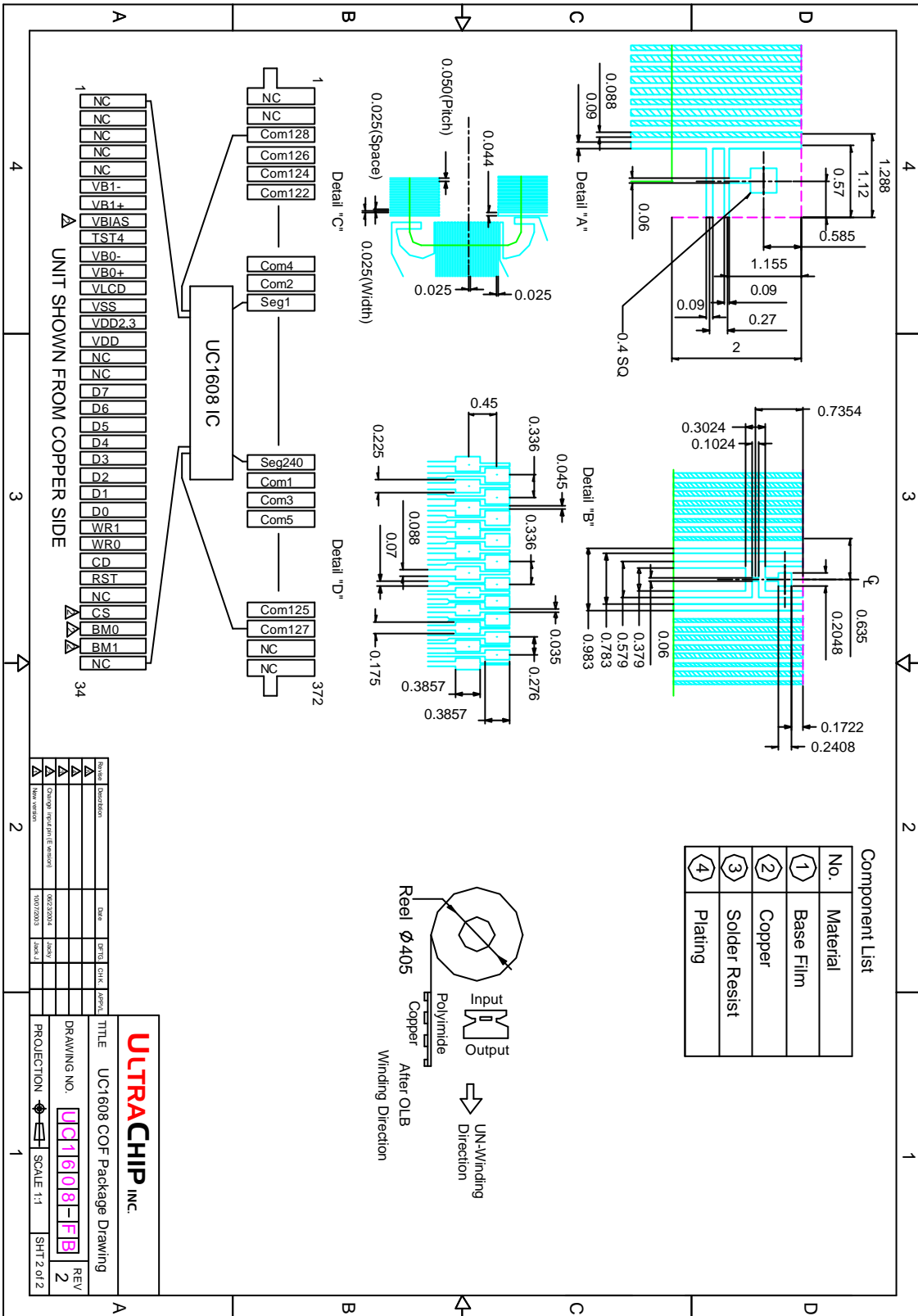
| Pin | Name   | X       | Y     | W    | H     |
|-----|--------|---------|-------|------|-------|
| 387 | SEG184 | -2857.5 | 577.6 | 27.0 | 112.0 |
| 388 | SEG185 | -2902.5 | 577.6 | 27.0 | 112.0 |
| 389 | SEG186 | -2947.5 | 577.6 | 27.0 | 112.0 |
| 390 | SEG187 | -2992.5 | 577.6 | 27.0 | 112.0 |
| 391 | SEG188 | -3037.5 | 577.6 | 27.0 | 112.0 |
| 392 | SEG189 | -3082.5 | 577.6 | 27.0 | 112.0 |
| 393 | SEG190 | -3127.5 | 577.6 | 27.0 | 112.0 |
| 394 | SEG191 | -3172.5 | 577.6 | 27.0 | 112.0 |
| 395 | SEG192 | -3217.5 | 577.6 | 27.0 | 112.0 |
| 396 | SEG193 | -3262.5 | 577.6 | 27.0 | 112.0 |
| 397 | SEG194 | -3307.5 | 577.6 | 27.0 | 112.0 |
| 398 | SEG195 | -3352.5 | 577.6 | 27.0 | 112.0 |
| 399 | SEG196 | -3397.5 | 577.6 | 27.0 | 112.0 |
| 400 | SEG197 | -3442.5 | 577.6 | 27.0 | 112.0 |
| 401 | SEG198 | -3487.5 | 577.6 | 27.0 | 112.0 |
| 402 | SEG199 | -3532.5 | 577.6 | 27.0 | 112.0 |
| 403 | SEG200 | -3577.5 | 577.6 | 27.0 | 112.0 |
| 404 | SEG201 | -3622.5 | 577.6 | 27.0 | 112.0 |
| 405 | SEG202 | -3667.5 | 577.6 | 27.0 | 112.0 |
| 406 | SEG203 | -3712.5 | 577.6 | 27.0 | 112.0 |
| 407 | SEG204 | -3757.5 | 577.6 | 27.0 | 112.0 |
| 408 | SEG205 | -3802.5 | 577.6 | 27.0 | 112.0 |
| 409 | SEG206 | -3847.5 | 577.6 | 27.0 | 112.0 |
| 410 | SEG207 | -3892.5 | 577.6 | 27.0 | 112.0 |
| 411 | SEG208 | -3937.5 | 577.6 | 27.0 | 112.0 |
| 412 | SEG209 | -3982.5 | 577.6 | 27.0 | 112.0 |
| 413 | SEG210 | -4027.5 | 577.6 | 27.0 | 112.0 |
| 414 | SEG211 | -4072.5 | 577.6 | 27.0 | 112.0 |
| 415 | SEG212 | -4117.5 | 577.6 | 27.0 | 112.0 |
| 416 | SEG213 | -4162.5 | 577.6 | 27.0 | 112.0 |
| 417 | SEG214 | -4207.5 | 577.6 | 27.0 | 112.0 |
| 418 | SEG215 | -4252.5 | 577.6 | 27.0 | 112.0 |
| 419 | SEG216 | -4297.5 | 577.6 | 27.0 | 112.0 |
| 420 | SEG217 | -4342.5 | 577.6 | 27.0 | 112.0 |
| 421 | SEG218 | -4387.5 | 577.6 | 27.0 | 112.0 |
| 422 | SEG219 | -4432.5 | 577.6 | 27.0 | 112.0 |
| 423 | SEG220 | -4477.5 | 577.6 | 27.0 | 112.0 |
| 424 | SEG221 | -4522.5 | 577.6 | 27.0 | 112.0 |
| 425 | SEG222 | -4567.5 | 577.6 | 27.0 | 112.0 |
| 426 | SEG223 | -4612.5 | 577.6 | 27.0 | 112.0 |
| 427 | SEG224 | -4657.5 | 577.6 | 27.0 | 112.0 |
| 428 | SEG225 | -4702.5 | 577.6 | 27.0 | 112.0 |
| 429 | SEG226 | -4747.5 | 577.6 | 27.0 | 112.0 |
| 430 | SEG227 | -4792.5 | 577.6 | 27.0 | 112.0 |
| 431 | SEG228 | -4837.5 | 577.6 | 27.0 | 112.0 |
| 432 | SEG229 | -4882.5 | 577.6 | 27.0 | 112.0 |
| 433 | SEG230 | -4927.5 | 577.6 | 27.0 | 112.0 |
| 434 | SEG231 | -4972.5 | 577.6 | 27.0 | 112.0 |
| 435 | SEG232 | -5017.5 | 577.6 | 27.0 | 112.0 |
| 436 | SEG233 | -5062.5 | 577.6 | 27.0 | 112.0 |
| 437 | SEG234 | -5107.5 | 577.6 | 27.0 | 112.0 |
| 438 | SEG235 | -5152.5 | 577.6 | 27.0 | 112.0 |
| 439 | SEG236 | -5197.5 | 577.6 | 27.0 | 112.0 |
| 440 | SEG237 | -5242.5 | 577.6 | 27.0 | 112.0 |
| 441 | SEG238 | -5287.5 | 577.6 | 27.0 | 112.0 |
| 442 | SEG239 | -5332.5 | 577.6 | 27.0 | 112.0 |
| 443 | SEG240 | -5377.5 | 577.6 | 27.0 | 112.0 |
| 444 | COM1   | -5422.5 | 577.6 | 27.0 | 112.0 |

**TRAY INFORMATION**



|                            |     |                |  |                |  |                |  |                |  |
|----------------------------|-----|----------------|--|----------------|--|----------------|--|----------------|--|
| Unless Otherwise Specified |     | Scale          |  | N/A            |  | Proj           |  | N/A            |  |
| Unit                       | mm  | Package Code   |  | N/A            |  |                |  |                |  |
| General Roughness          | N/A | Material       |  | N/A            |  |                |  |                |  |
| Tolerance                  |     | 2" IC Tray     |  |                |  |                |  |                |  |
| Type: H20-459x61-28(45)    |     | Drawn          |  | Checked        |  | Approved       |  | Drawing No.    |  |
| By: Jack Chung             |     | Date: 04-13-04 |  | By: Jack Chung |  | Date: 04-13-04 |  | 03-DWG-003-007 |  |
| Dimension drawing detail   |     | Date: 04-13-04 |  | Date: 04-13-04 |  | Date: 04-13-04 |  | 1 of 1         |  |
| Angle                      | N/A | Date: 04-13-04 |  | Date: 04-13-04 |  | Date: 04-13-04 |  | Sheet          |  |







## REVISION HISTORY

| Revision | Contents  | Date of Rev.  |
|----------|---|---------------|
| 0.6      | Golden Release  | Jul. 2, 2004  |
| 0.8      | (1) A constraint is added: To keep $V_{DD}$ and $V_{SS}$ under 150 O.<br>(Section "Reference COG Layout", page 7;<br>Section "ITO Layout Considerations", page 21)  | Jul. 30, 2004 |
|          | (2) Die size was changed to 11480 x 1375.<br>(Section "Revision History" – item 12, page 53)  |               |
|          | (3) The Revision records prior to ES revision are split into a separate file.<br>(Section "Revision History", page 53)  |               |
| 1.0      | (1) Some texts are marked bold to indicate default.<br>(Section "Control Registers", Pp 8~9;<br>"Command Description" – (5) Set Multiplex Rate, page 11;<br>"Command Description" - (19) Set LCD Bias Ratio, page 15) | Sep. 30, 2004 |
|          | (2) $V_{DD2/3}$ is corrected.<br>(Section "LCD Voltage Setting", page 16)   |               |
|          | (3) Note item 1, the recommended $C_{BIAS}$ range is adjusted:<br>50nF → 0.1 $\mu$ F<br>(Section " $V_{LCD}$ Quick Reference" – Hi-V Reference Circuit, page 19)  |               |
|          | (4) Some AC timings are adjusted.<br>(Section "AC Characteristics", Pp 39-40)   |               |
| 1.1      | (1) One more pin is added: $V_{DDX}$<br>(Section "Pin Description", page 6)   | Nov. 4, 2004  |
|          | (2) The COG drawing is updated: $V_{DD} \rightarrow V_{DDX}$<br>(Section "COG Reference Layout", page 7)  |               |
|          | (3) Pin 68 is renamed: $V_{DD} \rightarrow V_{DDX}$<br>(Section "Pad Coordinates", page 46)   |               |
|          | (4) In the "Operating Mode" table, the status of Draining Circuit in Sleep mode is corrected: "OFF" → "ON"  |               |
|          | (5) Most contents of sub-section "Changing Operation Mode" are re-written.<br>(Section "Reset & Power Management", page 33)   |               |
|          | (6) Sub-section "Extended Display OFF" is removed.  |               |
|          | (7) Sub-section "Brief Display OFF" is renamed as "Display OFF".<br>(Section "Reset & Power Management", page 36)   |               |
|          | (8) Average Frame Rate, $f_{FR}$ , is adjusted:<br>Max. : 84 → "-" (dash)<br>(Section "Specifications" – DC Characteristics, page 38)   |               |
|          | (9) A typo error is corrected: BR=11b → 10b   |               |
|          | (10) Test Condition (2) is removed.<br>(Section "Specifications" – Power Consumption, page 38)  |               |